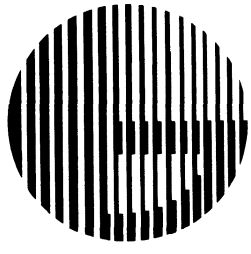
GENNUM
CORPORATION



designers and manufacturers of integrated circuit products with full inhouse capabilities for CAD/CAM, silicon process, testing, packaging and applications assistance.

1989 PRODUCT CATALOG

GENNUM CORPORATION, P.O.Box 489, Station A, Burlington Ontario, Canada L7R 3Y3
Tel.(416) 632-2996 Fax:(416) 632-2055 Telex:061-8525

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Excellence Through People and Technology!

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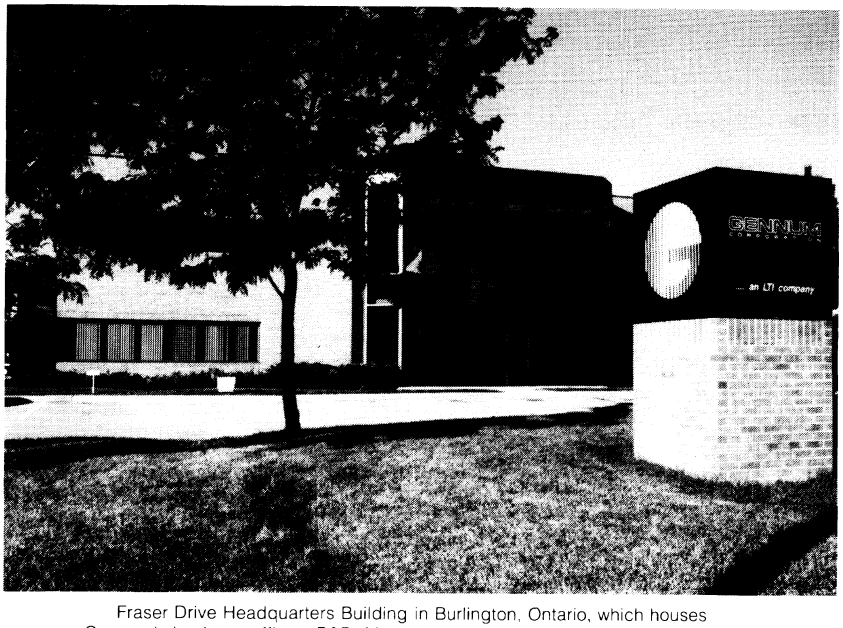


Fraser Drive Headquarters Building in Burlington, Ontario, which houses Gennum's business offices, R&D, Marketing, Masking, Test and Assembly areas.

The Landmark Road facility, also in Burlington, Ontario, where all the silicon processes are located.

Gennum Corporation supplies electronic components to manufacturers of electronic systems all over the world. Our business is the design, manufacture and marketing of silicon integrated circuits, (ICs). Employing over 200 people, Gennum is housed in two modern facilities in Burlington, Ontario, just a few miles west of Toronto. A recent addition is the opening of an office in Tokyo, Japan. To better serve our worldwide customers Gennum has 31 agents and/or design centres in 14 countries.

Gennum Corporation, created in 1987, continues the integrated circuit operations, conducted since 1973, by LTI, Gennum's parent company. This business which Gennum Corporation continues has grown to some twenty two million dollars of sales in 1988, sharing in the tremendous growth which has been experienced in electronic component manufacturing since 1973.

Gennum's continued growth has occurred because of a business philosophy: - attention to individuals' needs; customers, suppliers, employees and investors alike.

Capabilities in terms of human and physical resources extend through all facets of the company. These include technology development, new product design and development, and all aspects of wafer fabrication, device assembly and testing. Skills and abilities are constantly improved through the application of the latest tools and technologies applied to new products and existing products alike. This gives Gennum customers the competitive advantage essential to their success.

Currently Gennum Corporation serves five distinct areas within the electronic systems and subsystems market.

- resonant mode controller ICs for power supplies,
- crosspoint switches for the video/broadcast industry
- special application products
- semicustom IC linear arrays
- low voltage, low current BiFET products such as amplifiers and filters.

This comprehensive catalog provides detailed information on products in all five areas, with data sheets, application notes, and packaging information. Applications assistance is available at any time from our applications engineers.

Corporate Mission:

Excellence Through People and Technology!

- serve the customer
- respect people
- pursue excellence

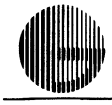
The exacting processes of integrated circuit design and production force a hard discipline on those who manufacture them and Gennum Corporation is no exception to this rule.

The company's silicon processing includes linear bipolar producing circuits with operating ranges from as low as 1.0V up to 30V and transistor current handling capability up to 3A. In combination with the above, ion implanted JFETs and Schottky diodes can be added.

To help us stay in the forefront of technology, Gennum maintains affiliations with the scientific and engineering departments of five Canadian universities.

Computer aided design is a major component of our product development cycle. The highly efficient equipment and personnel are able to shorten design time and cost while increasing reliability. Simulation programs such as SPICE, SUPREM and COMPACT are available in-house for design optimization. Their use allows investigation of circuit performance under the most extreme cases of device matching and over as wide a range of temperature as necessary.

To ensure that every product meets Gennum's high quality standards, we perform in-line sample inspection on each batch from incoming inspection, to the final test of the finished product. Gennum's entire manufacturing process is governed by strict production controls performed by production personnel, as well as quality control audit inspections to double check the quality practices instituted by other groups.



SELLING POLICY

GENNUM CORPORATION

GENNUM 010

G
2

1. Order Acceptance

No order is contractually binding on Gennum Corporation unless accepted in writing by an authorized representative of the Company. All orders are accepted in accordance with the terms outlined herein notwithstanding any conflicting terms which may appear on the Buyer's order.

Orders will be accepted for:

1.1 Complete delivery in a single shipment on a specific date. These are called Single Shipment Orders.

1.2 Delivery in many shipments spread over an extended period. These are called Extended Period Blanket (EPB) Orders.

2. Contractual Period

2.1 A purchase order which has been accepted in accordance with Paragraph 1 above, will be contractually binding on both Seller and Buyer for the contractual period, which lasts from the date of first shipment to the date on which the total quantity of units ordered has been shipped by the Seller or for twelve months, whichever comes first.

2.2 The contractual period may be extended beyond the twelve month limit provided both Buyer and Seller agree so to do in writing.

3. Prices

Prices shown on a quotation will remain firm for the validity period of the quotation. Prices shown on an order acknowlegement will remain firm during the contractual period, except that a price decrease which is freely offered by the Seller will apply to all shipments made after its effective date.

4. Termination of an Order

An order shall be automatically terminated at the end of the contractual period. The Buyer may terminate an order prematurely by providing the Seller with 60 days notice in writing. In the event of premature termination the following shall apply.

4.1 The Seller is entitled to ship all parts which were previously scheduled for shipment before termination date by the Buyer.

and

4.2 The Buyer is liable for payment for all parts shipped in accordance with Paragraph 4.1 above, including additional payments arising from increased per unit prices at the reduced quantity. The Buyer is liable for back billing for all parts shipped at the applicable blanket order prices.

and

4.3 Payment of a reasonable charge based upon expenses incurred and commitments made in the execution of the purchase contract by Gennum Corporation up to the date of receipt of the notice of termination; the charge being a minimum of 15% of the unrealized invoice value of the order.

5. Extended Period Blanket (EPB) Orders

5.1 EPB Orders will be accepted for any products in quantities to cover expected requirements over the contractual period. The total of all products ordered may be used to determine the per unit price of each proprietary product accordance with the quotation submitted by the Seller to the Buyer.

5.2 Changes to EPB orders by the Buyer, including changes in device types ordered, and changes in order quantity, either decrease or increase, will be accepted by the Seller subject to the following limitations:

5.2.1 Within 3 months from date of order acceptance, a change in total quantity ordered, either an increase or decrease, which results in the total number of units being in a different price/quantity range, will automatically change the per unit price for all prior and subsequent shipments.

5.2.2 At any time after order acceptance, changes in device types ordered, either by addition, deletion, or substitution, shall at the discretion of the Seller, require sixty days notice in writing.

6. Shipping Schedule

Unless purchase orders are accompanied by a shipping schedule, shipment will be at the Seller's discretion. In the case of Extended Period Blanket Orders, the order must be accompanied by a shipping schedule which releases at least 40% of the total order quantity for shipment in a period not to exceed five months from the beginning of the contractual period. The remaining parts on a EPB order may be released at the Buyer's discretion provided:

6.1 All parts are scheduled for **shipment** within the Contractual Period.
and
6.2 The Buyer provides the Seller with at least 12 weeks notice of any new shipping requirement or amendment to existing shipping schedule.

7. Terms of Payment

The terms of payment agreed between the Seller and Buyer will be clearly shown on the Order Acceptance document supplied by the Seller to the Buyer. Until credit terms have been negotiated, the only terms of payment which will be accepted by the Seller are cash with order. Gennum Corporation reserves the right to apply a monthly service charge not in excess of two percent per month, on the overdue payment balance, provided it supplies the Buyer with thirty days notice in writing.

8. Loss or Damage in Transit or Short Shipment

All shipments should be inspected by the Buyer immediately upon receipt. If there is evidence of loss or damage during transit, the Buyer should immediately file a claim with the carrier. Gennum Corporation will cooperate with the Buyer to ensure that a proper adjustment with the carrier is obtained. In the event of short shipment, claims must be made directly to Gennum Corporation in writing within fifteen working days after receipt of goods.

9. Warranty

Gennum Corporation warrants that its products will be free of defects in material and workmanship and will perform as specified in the governing data sheet for one year from date of shipment. The liability of Gennum Corporation is limited to repairing, replacing F.O.B. Burlington, Ontario, Canada, products which are returned by the Purchaser at **his expense** during the warranty period. Final determination as to whether a product is actually defective rests with Gennum Corporation. This warranty shall automatically become null and void if the products are used in an unreasonable manner or in a manner which exceeds the absolute maximum ratings specified by the governing data sheet.

9.1 Returns - Warranty

An RMO number and authorization must be obtained from Gennum Corporation before material is returned.

9.1.1 If an entire shipment is being returned based on a Quality Assurance Sampling Process, the defective devices must first be sent to Gennum Corporation for confirmation. Once confirmed, the entire shipment may be returned, following normal procedures. Devices which have been used or subjected to any production process are not eligible for credit.

9.2 Non-Warranty

Any product returned for reasons other than defective must receive an RMO number and authorization and will be subject to a restocking charge.

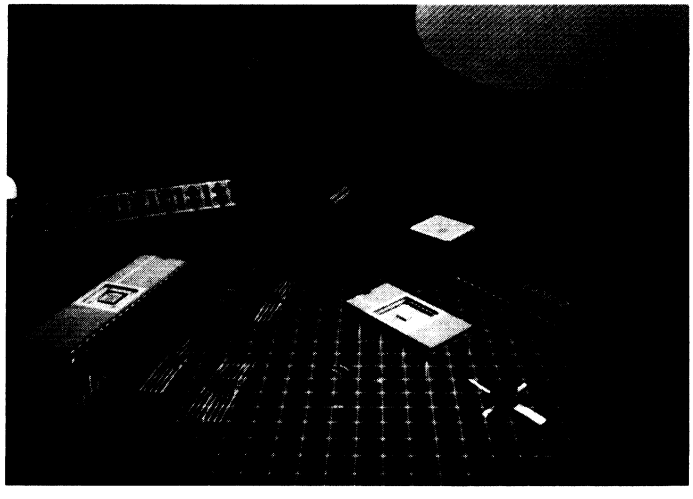
10. Limitation of Liability

Notwithstanding any other provision in this contract or any applicable statutory provisions, neither Gennum Corporation nor the purchaser shall be liable to the other for special or consequential damages or damages for loss of use arising directly or indirectly from any breach of this contract (fundamental or otherwise) or from any tortius acts or omissions of their respective employees or agents and in no event shall the liability of Gennum Corporation exceed the unit price of the product.

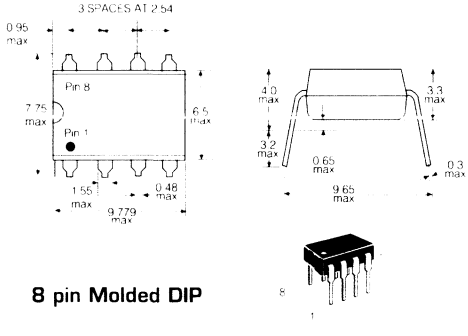
11. Force Majeure

Gennum Corporation shall not be responsible or liable for any loss, damage, detention or delay caused by war, invasion, insurrection riot, the order of any civil or military authority, or by fire, flood, weather or other acts of the elements, breakdown, lockouts, strikes or labour disputes, the failure of its suppliers to meet their contractual obligations, or, without limitation of the foregoing, any other cause beyond its reasonable control and the receiving of the product by the Purchaser shall constitute a waiver of all claims for loss or damage due to delay.

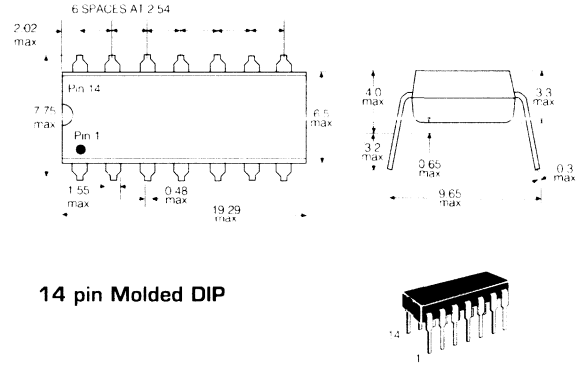
AVAILABLE PACKAGING



Gennum can provide a wide variety of proprietary and standard packages.



8 pin Molded DIP

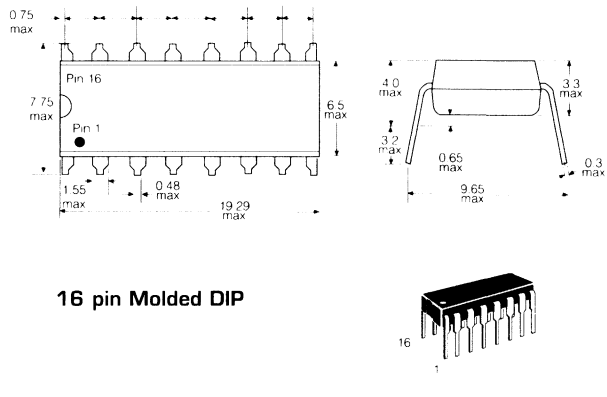


14 pin Molded DIP

Other standard DIP packaging is available for custom and semicustom products.

STANDARD DIP PACKAGES

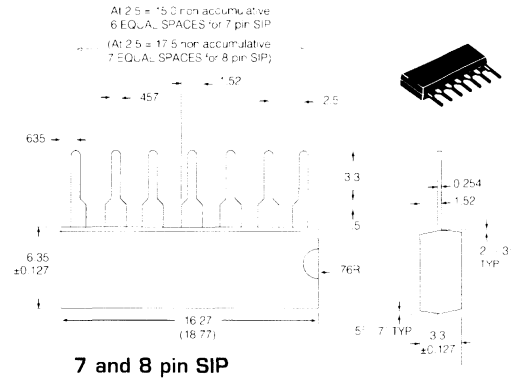
All dimensions in millimetres



16 pin Molded DIP

OTHER STANDARD PACKAGING

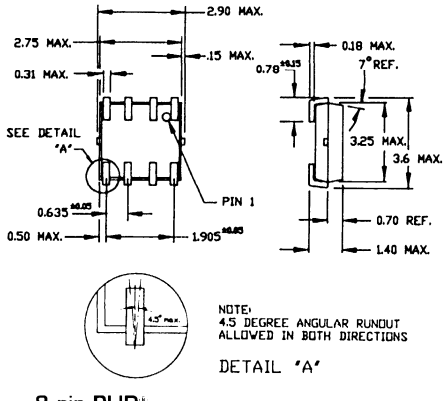
All dimensions in millimetres



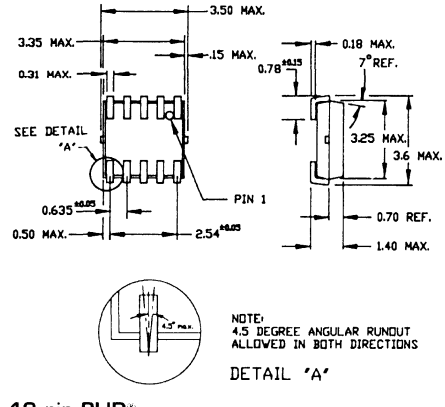
7 and 8 pin SIP

GENNUM PROPRIETARY PACKAGING

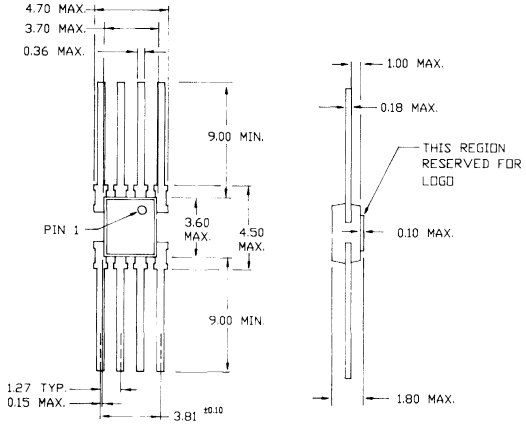
All dimensions in millimetres



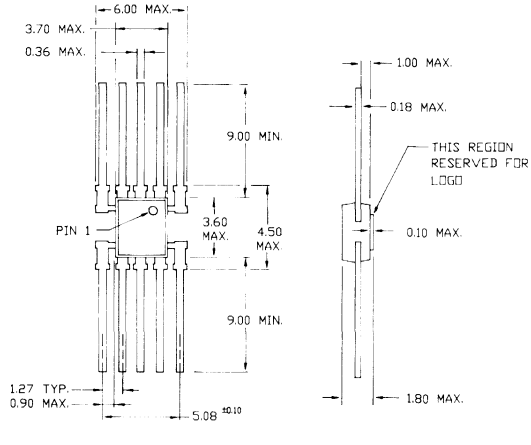
8 pin PLID*



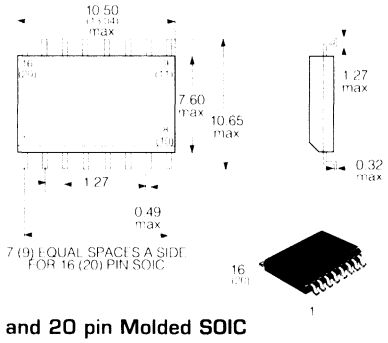
10 pin PLID*



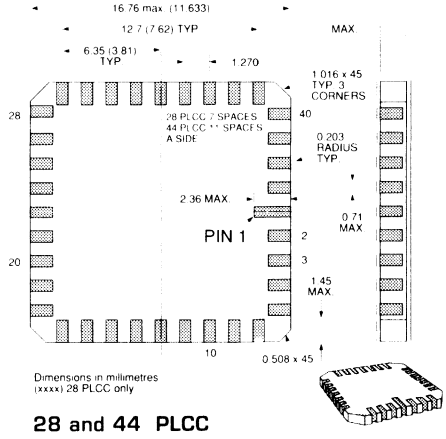
8 pin MINIpac



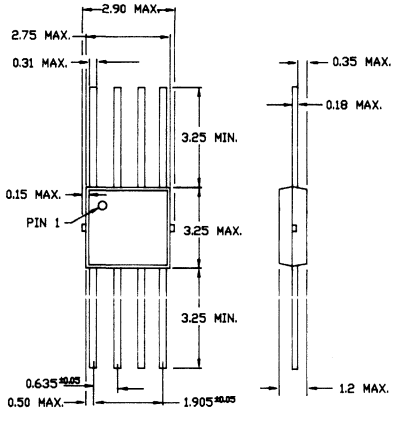
10 pin MINIpac



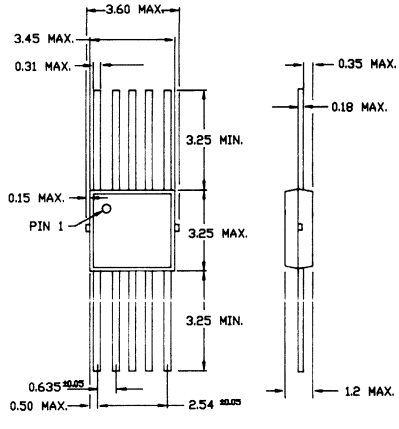
16 and 20 pin Molded SOIC



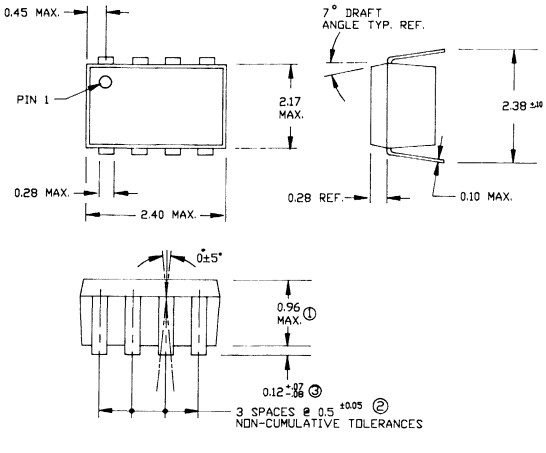
28 and 44 PLCC



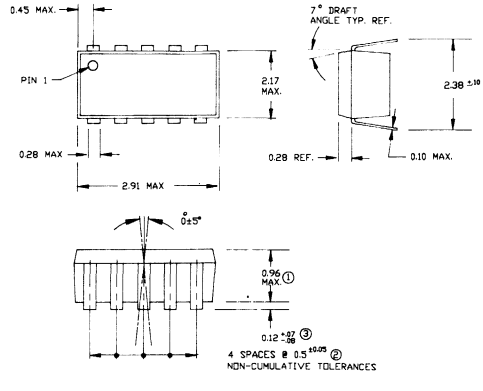
8 pin MICROpac



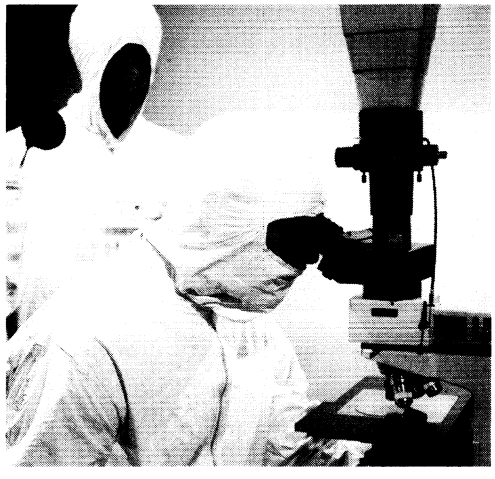
10 pin MICROpac



8 pin SLT



10 pin SLT



Wafer Inspection

Automated Test Equipment and DIP Handler

RELIABILITY THROUGH QUALITY

- **Procedures designed to meet MIL-STD105D**
- **Quality audits**
- **All employees participate in the "Quality Improvement Process"**
- **Products are sampled for reliability at all stages of manufacture.**

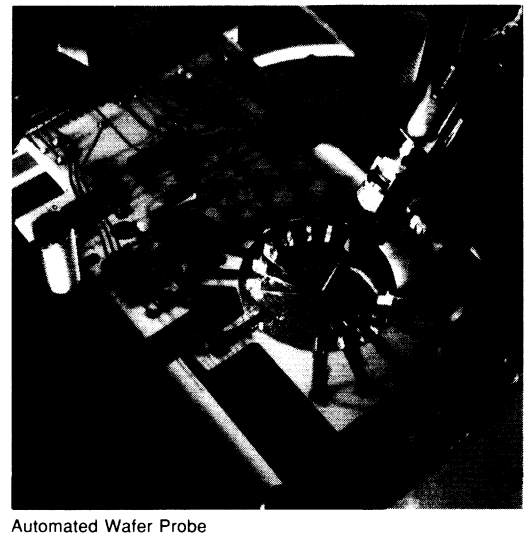
QUALITY POLICY

"In all activities
- *know the job requirements,*
- *set standards to meet requirements,*
- *conform to standards."*

Quality is not just the concern of the production area at Gennum. All departments and employees are participants in the quality program and each has responsibilities which could affect the other. Therefore, with this obligation in mind a *total quality tradition* is a viable program which works for all aspects of the company, be it design, production, marketing and sales, or administration and finance.

Performance indicators and goals are monitored constantly and variances are analyzed using techniques such as Pareto, cause/effect, Taguchi methods and brainstorming.

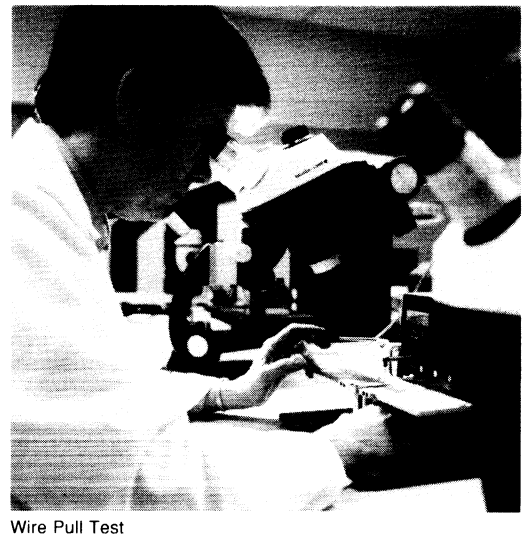
Throughout the wafer fabrication and chip assembly areas, statistical process control charts are used to monitor the consistency of all parameters and the quality of all products as they move from operation to operation. Products are one hundred per cent electrically tested twice during manufacture. Other types of testing are done on a sample basis both in-house and by outside, independent testing laboratories.



Automated Wafer Probe

IN-LINE QUALITY CONTROL

At Gennum we maintain inspections and statistical process controls at numerous key points , from incoming material, through to the tested and packaged product. All our visual inspection is conducted to MIL-STD 883, class B requirements.



Wire Pull Test

QUALIFICATION

The purpose of qualification is to ensure that only reliable products will be introduced into the manufacturing stage, and ultimately reach the marketplace.

Two levels of qualification test routines are performed on all new product designs at Gennum.

1. Initial Qualification from Design to Preproduction

- representative sample
- attribute tests
- high temperature storage
- temperature shocks
- attribute tests
- report

2. Follow-up Qualification from Preproduction to Production

- representative sample
- attribute tests
- high temperature burn-in
- temperature cycle
- attribute tests
- pressure cook/temperature humidity bias (95°C / 95%RH)
- attribute tests
- report

CALIBRATION

A calibration program has been established which covers all equipment used to design, manufacture, test and inspect products. This program is traceable to national standards.

QUALITY LEVELS

Quality means conformance to defined specifications and standards, through measureable and monitable parameters.

At the output of Silicon Operations, and Assembly Operations, Quality Assurance gates have been established to ensure that in-line systems are effectively producing products which conform to specifications.

All finished devices are subject to both mechanical and electrical inspection based in MIL STD 105D sampling plans. All outgoing inspection data is analyzed so as to monitor outgoing quality performance.

Gennum is committed to reduce AOQ (Average Outgoing Quality) levels by one half each year and so minimize customer returns.

AOQ	1988	1989	1990	1999
	0.05%	0.03%	0.018%	0.01%

The Ultimate Goal: Zero Defects

Environmental Lab

Q.A. Station

VIDEO & BROADCAST PRODUCTS

VBD data sheets

VBA application notes

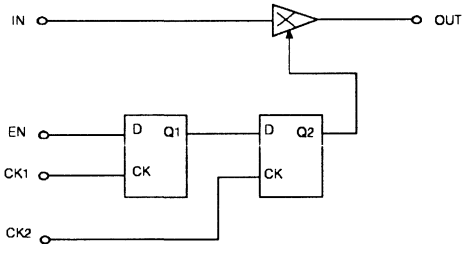
Monolithic 1x1 Video Crosspoint Switch with Two Latches

GX411 PRELIMINARY DATA SHEET

FEATURES

* differential gain at 3.58 MHz, 0.05% (max.)
* differential phase at 3.58 MHz, 0.025 deg.(max.)
* dual latches
* off-isolation at 10 MHz, 90 dB (min.)
* -3 dB bandwidth, 100 MHz (min.)
* insertion loss at 100 kHz, 0.03 dB (typ.)

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

EN	CK1	CK2	Q1	Q2
0	1	0	0	$Q2_{n-1}$
0	1	1	0	0
1	1	0	1	$Q2_{n-1}$
1	1	1	1	1
X	0	0	$Q1_{n-1}$	$Q2_{n-1}$
X	0	1	$Q1_{n-1}$	$Q1_{n-1}$

X = DON'T CARE

Q2	OUT
0	HIGH Z
1	IN

ORDERING INFORMATION

Part Number	Package	Temperature Range
GX411 CS	8 pin SIP	0°C to 70°C

CIRCUIT DESCRIPTION

The GX411 is a broadcast quality 1x1 video crosspoint featuring two control latches, implemented in bipolar monolithic technology. The device is characterized by low differential gain and phase, extremely high off isolation, and a -3 dB bandwidth of 100 MHz.

For use in NxM routing matrices, the GX411 features very high output impedance in the disabled state. This allows multiple devices to be paralleled at the input and output without additional circuitry. A fully buffered unilateral signal path ensures negligible output to input feedback while delivering minimal output switching transients through make-before-break switching.

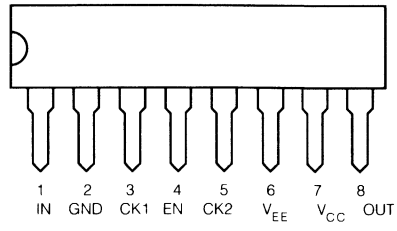
To maximize system bandwidth, an external current source is used to bias the output device of the crosspoint. One external current source is required per output bus. For less demanding applications, a load resistor can be used in place of the output current source, causing a slight increase in differential phase. Non-additive mixing will occur on the output bus if more than one paralleled GX411 is enabled at a time.

Dual transparent latches allow asynchronous addressing and synchronous switching. The control microprocessor can write to the input latch using *CK1*, while the video timing clock can be used to initiate switching using *CK2*. Alternatively, one or both of the latches can be made transparent by pulling *CK1* or *CK2* high.

The device operates over a supply voltage range from ±7 to ±13.2 volts. With a supply voltage of ±8 V, the device dissipates only 8 mW in the disabled state.

APPLICATIONS

- video routing switchers
- video production and master control switchers
- CCTV / CATV



PIN CONNECTION
8 PIN SIP

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ABSOLUTE MAXIMUM RATINGS

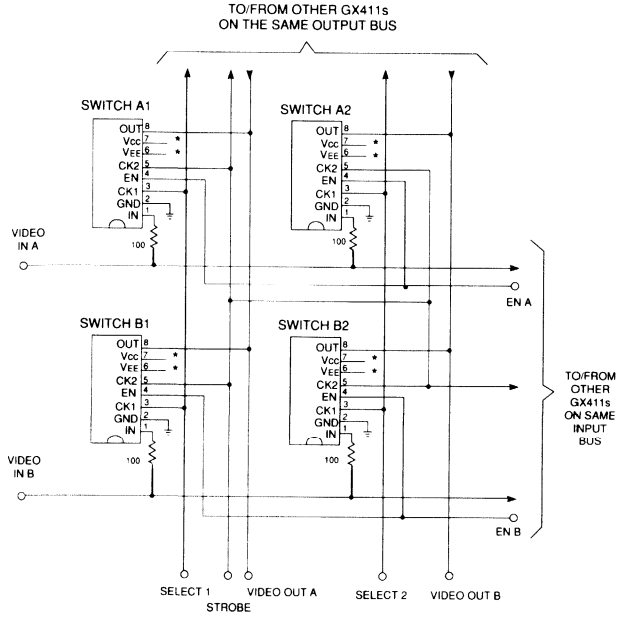
Parameter	Value
Supply Voltage	±13.5 V
Operating Temperature Range	0 °C ≤ T_A ≤ 70 °C
Storage Temperature Range	-65 °C ≤ T_S ≤ 150 °C

Parameter	Value
Lead Temperature (Soldering, 10 Sec)	260 °C
Analog Input Voltage	-5 V ≤ V_{IN} ≤ V_{CC}+0.3 V or V_{EE} +20 V
Logic Input Voltage	0 V ≤ V_L ≤ 5.5 V

ELECTRICAL CHARACTERISTICS (V_S = ±8 V DC, 0°C < T_A < 70 °C, R_L = 10 kΩ, C_L = 30pF, I_L = 2 mA)

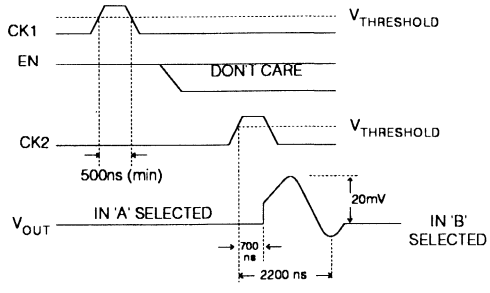
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	$\pm V_S$		7	8	13.2	V
	Supply Current (I_L of 2 mA not included)	I+	Q2 = 1	-	9.7	12.6	mA
			Q2 = 0	-	0.45	0.59	mA
		I-	Q2 = 1	-	9.5	12.4	mA
			Q2 = 0	-	0.38	0.5	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2	-	5.5	V
	Analog Input Bias Current	I_{BIAS}		-	20	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25 °C	-10	-	10	mV
	O/P Offset Voltage Drift	$\Delta V_{OS} / \Delta T$		-	50	200	µV / °C
LOGIC	Crosspoint selection Turn-on time	t_{ON}	From CK2	-	0.7	-	µs
			From EN	-	0.8	-	
	Crosspoint selection Turn-off time	t_{OFF}	From CK2	-	2.2	-	µs
			From EN	-	2.4	-	
	Clock Pulse Width	t_{CK}		500	-	-	ns
	Logic Input Thresholds	V_{IH}	1	2.0	-	-	V
		V_{IL}	0	-	-	1.1	V
	Enable Input Bias Current	$I_{BIAS(EN)}$	EN=1	-	0.5	3.0	µA
	CK1/CK2 Bias Current	$I_{BIAS(CK)}$	CK1/CK2=0	-	0.7	5.0	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.02	0.03	0.05	dB
	Bandwidth (-3dB)	B.W.		100	-	-	MHz
	Gain Spread at 8 MHz			-	-	±0.06	dB
	Input Resistance	R_{IN}	Chip selected	1	-	-	MΩ
	Input Capacitance	C_{IN}		-	2	-	pF
	Output Resistance	R_{OUT}		-	15	-	Ω
	Output Capacitance	C_{OUT}		-	3.5	-	pF
	Differential Gain	dg	at 3.58 MHz V_{IN} = 40 IRE	-	-	0.05	%
	Differential Phase	dp		-	-	0.025	deg
	Off Isolation		Crosspoint on output to gnd. f = 10 MHz	90	100	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	120	190	-	V/µs
		-SR		110	170	-	

Fig. 1 Typical Application Circuit of Four GX411's Connected as a 2x2 Matrix.



* For purposes of clarity, all supply pins are not shown connected together.
Each V_{CC} and V_{EE} pin should be decoupled with a 0.1µF capacitor.

Fig. 2 Typical Crosspoint Timing Diagram



CAUTION
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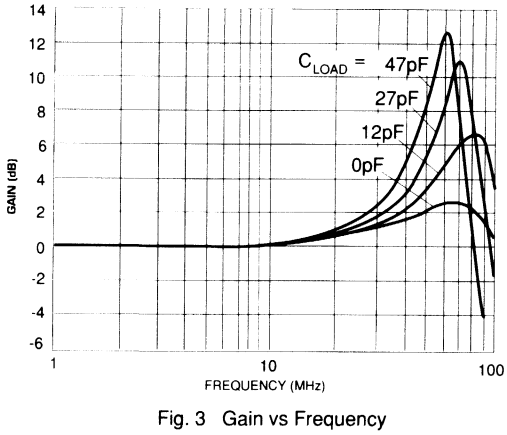


Fig. 3 Gain vs Frequency

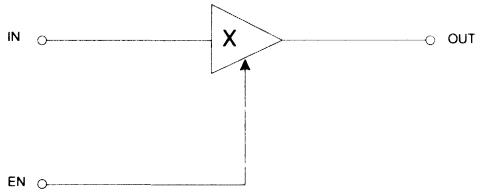
Wideband, Monolithic 1x1 Video Crosspoint Switch

GX4101 TENTATIVE DATA SHEET

FEATURES

* differential phase and gain at 3.58 MHz, 0.01° & 0.01% (max.)
* -3 dB bandwidth, 300 MHz (typ.) with C_L = 0 pF
* off isolation at 100 MHz, 80 dB (typ.)
* ±4.5 V to ±13.2 V power supplies
* low disabled power dissipation, 0.8 mW at V_S = ±5 V
* input signal levels from -2.4 V to +3.0 V
* logic input compatible with TTL and 5 V CMOS

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

EN	OUT
0	HIGHZ
1	IN

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5 V
Operating Temperature Range	0° C ≤ T_A ≤ 70° C
Storage Temperature Range	-65° C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	-4 V ≤ V_{IN} ≤ 3 V
Logic Input Voltage	0 V ≤ V_L ≤ 5.5 V

CIRCUIT DESCRIPTION

The GX4101 is a wideband 1x1 video crosspoint implemented in bipolar monolithic technology. The device is characterized by excellent differential gain and phase in the enabled state, and very high off-isolation in the disabled state. The fully buffered unilateral signal path ensures negligible output to input feedback while delivering minimal output switching transients through make-before-break switching.

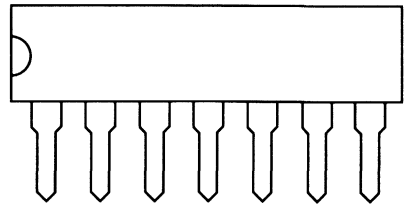
For use in NxM routing matrices, the device features a very high, nearly constant input impedance, coupled with very high output impedance in the disabled state. This allows multiple GX4101's to be paralleled at the input and output without additional circuitry.

To maximize system bandwidth, an external current source is used to bias the output device of the crosspoint. One external current source is required per output bus. For less demanding applications, a load resistor can be used in place of the output current source, causing a slight increase in differential phase. Non-additive mixing will occur on the output bus if more than one paralleled GX4101 is enabled at a time.

The GX4101 is the first in a series of wideband video crosspoints utilizing Gennum's proprietary LSI process.

APPLICATIONS

* very high quality video switching
* computer graphics
* high definition TV
* RF switching/routing
* PCM/data routing



PIN CONNECTION
7 PIN SIP

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-Ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, I_L = 3 mA)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	Supply Voltage	$\pm V_S$		±4.5		±13.2	V
DC SUPPLY	Supply Current (not including external current load)	I+	EN=1	-	2	-	mA
			EN=0	-	100	-	µA
		I-	EN=1	-	1.9	-	mA
			EN=0	-	60	-	µA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2.4	-	3.0	V
	Analog Input Bias Current —	I_{BIAS}		-	5	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25°C	-10	-	10	mV
LOGIC	Output Offset Voltage Drift-	$\Delta V_{OS} / \Delta T$		-	15	60	µV/°C
	Crosspoint Turn-On Time	t_{ON}	Control input to appearance of signal at output.	-	100	200	ns
	Crosspoint Turn-Off Time	t_{OFF}	Control input to disappearance of signal at output.	0.5	1.0	-	µs
	Logic Input	V_{IH}	1	2.0	-	-	V
	Thresholds	V_{IL}	0	-	-	1.1	V
	Enable Bias Current	$I_{BIAS(EN)}$	EN = 1	-	-	0.5	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	-	0.05	-	dB
	Bandwidth (-3dB)	B.W.	small signal C_L = 0 pF	-	300	-	MHz
	Input Resistance	R_{IN}	EN = 0	1.0	-	-	MΩ
	Input Capacitance	C_{IN}	EN = 1	-	2	-	pF
	Output Resistance	R_{OUT}	EN = 1	-	14	-	Ω
	Output Capacitance	C_{OUT}	EN = 0	-	4	-	pF
	Differential Gain	dg	at 3.58 MHz	-	-	0.01	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	-	0.01	degrees
	Off Isolation		Enabled GX4101 on output f = 100 MHz	-	80	-	dB
	Slew Rate	+SR		100	-	-	
		-SR	V_{IN} = 3V p-p (C_L = 0 pF)	100	-	-	V/µs

AVAILABLE PACKAGING

7 pin SIP

CAUTION
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SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC FREE WORKSTATION

Monolithic 1x1 Video Crosspoint Switch

GX401 DATA SHEET

VBD 3

FEATURES

* 100 MHz bandwidth (-3 dB)
* insertion loss 0.03dB at 100 kHz
* gain spread ±0.075dB at 8 MHz
* differential gain at 3.58 MHz 0.04% (max)
* differential phase at 3.58 MHz 0.02° (max)
* TTL and 5 V CMOS compatible logic inputs
* compatible with all popular video standards
* 7 pin single-in-line package
* built-in enable latch allows synchronous selection

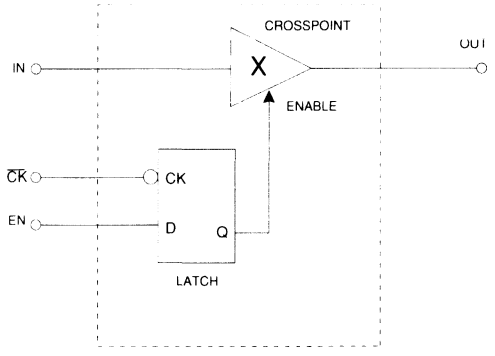
CIRCUIT DESCRIPTION

The GX401 is a low cost monolithic 1x1 video crosspoint switch plus on-board latch, designed primarily for use in video switching applications where 1 out of N channel selection function is required. Unlike similar devices using MOS bilateral switching elements, the GX401 represents a fully buffered unilateral transmission path when enabled, and offers better than 90 dB of off isolation at 10 MHz when disabled.

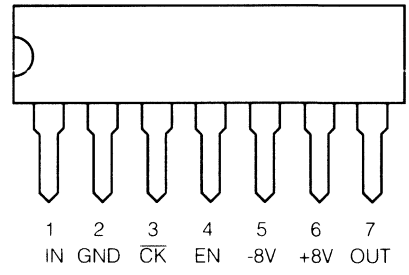
In addition, the GX401 offers wide bandwidth and superior differential gain and phase performance.

Power supply requirements are ±8 volts. Logic inputs are TTL and 5V CMOS compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±10.0 V
Operating Temperature Range	$0° C \le T_A \le 70° C$
Storage Temperature Range	$-65° C \le T_S \le 150° C$
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	$-4 V \le V_{IN} \le 2.4 V$
Logic Input Voltage	$-4 V \le V_L \le 5.25 V$

NOTE: Output is not short circuit protected.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX401CS	7 Pin SIP	0° to 70°C

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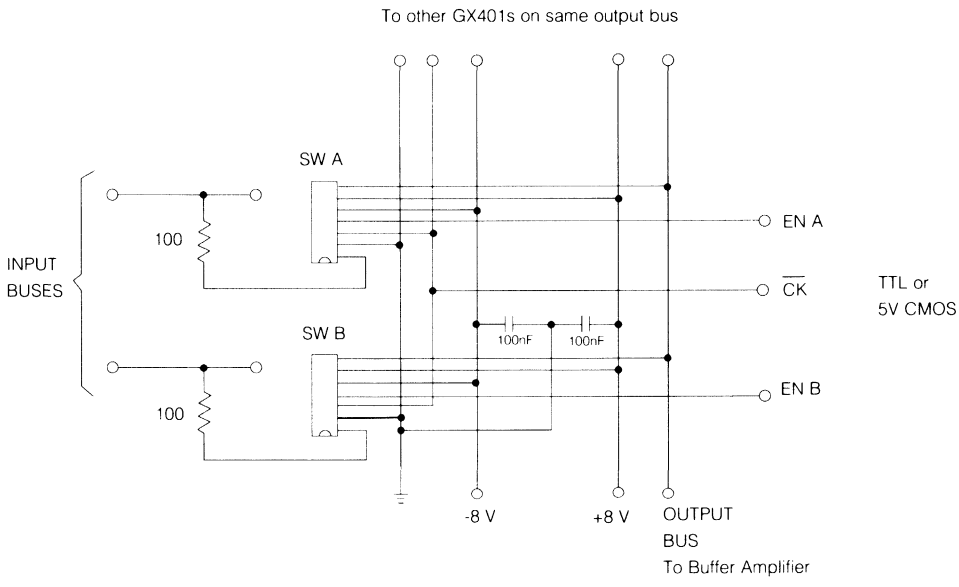
ELECTRICAL CHARACTERISTICS (V_S = ±8V DC. 0°C < T_A < 70°C, R_L = 10kΩ, C_L = 30pF. Typical values are at T_A=25°C)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	Supply Voltage	V_S ±		7.5	8.0	8.5	V
DC		I+	Chip selected (EN=1)	-	15	18	mA
SUPPLY			Chip not selected (EN=0)	-	0.7	0.9	mA
	Supply Current	I-	Chip selected (EN=1)	-	14	17	mA
			Chip not selected (EN=0)	-	0.63	0.85	mA
	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-1.2	-	+2.0	V
STATIC	Output Offset Voltage	V_{OS}	75Ω resistor on each input to gnd	5	15	25	mV
	Output Offset Voltage Drift-	ΔV_{OS} / ΔT		-	50	200	µV/°C
	Crosspoint Turn-On Time	t_{ON}	Control input to appearance of signal at output.	300	400	500	ns
	Crosspoint Turn-Off Time	t_{OFF}	Control input to disappearance of signal at output.	900	1200	1600	ns
	Clock input Pulse width	t_{CK}	Control input to appearance of signal at output	350	-	-	ns
LOGIC	Logic Input	V_{IH}	1	2.0	-	-	V
	Thresholds	V_{IL}	0	-	-	0.8	V
	Enable	$I_{BIAS(EN)}$	EN = 1	-	-	2.0	µA
	Bias Current		EN = 0	-	-	-0.1	µA
	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.02	0.03	0.05	dB
	Bandwidth (-3dB)	B.W.		100	-	-	MHz
	Gain Spread at 8 MHz			-	-	±0.075	dB
	Input Resistance	R_{IN}	Chip selected (EN = 1)	900	-	-	kΩ
DYNAMIC	Input Capacitance	C_{IN}	Chip selected (EN = 1)	-	2.0	-	pF
			Chip not selected (EN = 0)	-	2.2	-	pF
	Output Resistance	R_{OUT}	Chip selected (EN = 1)	-	12	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected (EN = 0)	-	7	-	pF
	Differential Gain	dg	f = 3.58 or 4.43 MHz	-	0.03	0.04	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	0.01	0.02	degrees
	Off Isolation		Crosspoint on output to gnd. f = 10 MHz	90	-	-	dB

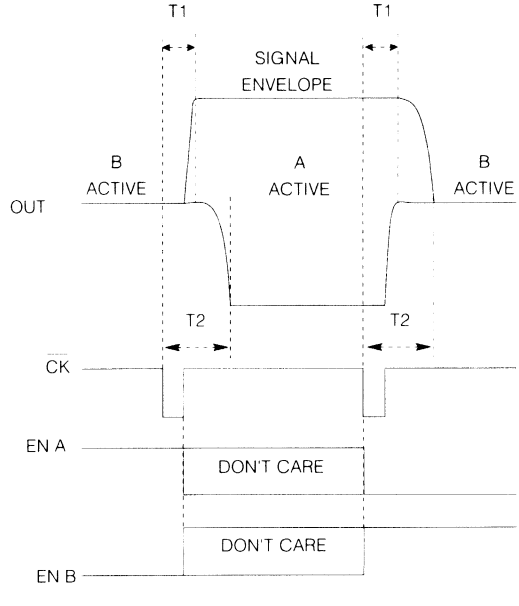
AVAILABLE PACKAGING

7 pin SIP

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC FREE WORKSTATION



TYPICAL GX401 APPLICATION CIRCUIT



CONDITIONS:
Input B: grounded via 75Ω
Input A: 1V p-p sinewave
T1 = 400 ns
T2 = 1.2 µs

NOTE:
Clock is level triggered

TYPICAL CROSSPOINT SELECTION TIMING DIAGRAM

Monolithic 4x1 Video Crosspoint Switches

GX414, GX424, GX434 DATA SHEET

VBD 4

FEATURES

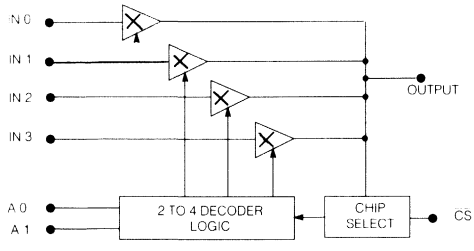
- **low differential gain: 0.03% typ. at 4.43 MHz**
- **low differential phase: 0.012 deg. typ. at 4.43 MHz**
- **low insertion loss: 0.05 dB max at 100 kHz**
- **low disabled power consumption: 5.2 mW typ.**
- **high off isolation: 110 dB at 10 MHz**
- **all hostile crosstalk @ 5 MHz, 97 dB typ.**
- **bandwidth (-3dB) with 30 pF load, 100 MHz typ.**
- **fast make-before-break switching: 200 ns typ.**
- **TTL and 5 volt CMOS compatible logic inputs**
- **low cost 14 pin DIP and16 pin SOIC packages**
- **optimised performance for NTSC, PAL and SECAM applications**

APPLICATIONS

Glitch free analog switching for...

- High quality video routing
- A/D input multiplexing
- Sample and hold circuits
- TV/ CATV/ monitor switching

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

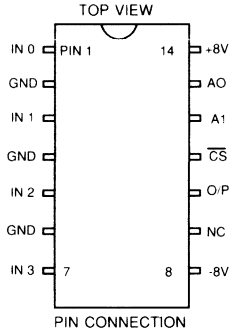
X = DON'T CARE

CIRCUIT DESCRIPTION

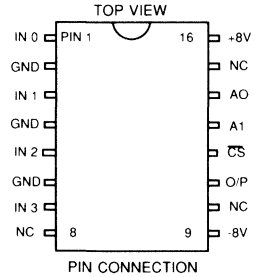
The GX414, GX424 and GX434 are high performance low cost monolithic 4x1 video crosspoints incorporating four bipolar switches with a common output, a 2 to 4 address decoder and fast chip select circuitry. The chip select input allows for multi-chip paralleled operation in routing matrix applications. The chip is selected by applying a logic 0 on the chip select input.

Unlike devices using MOS bilateral switching elements, these bipolar circuits represent fully buffered, unilateral transmission paths when selected. This results in extremely high output to input isolation. They also feature fast make-before-break switching action. These features eliminate such problems as switching 'glitches' and output-to-input signal feedthrough.

This family of devices operates from ±7 to ± 13.2 volt DC supplies. They are specifically designed for video signal switching which requires extremely low differential phase and gain. Logic inputs are TTL and 5 volt CMOS compatible providing address and chip select functions. When the chip is not selected, the output goes to a high impedance state.

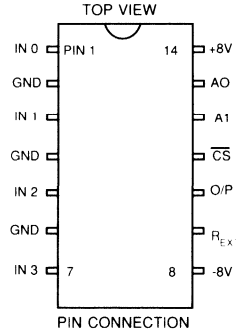


PIN CONNECTION
14 PIN DIP

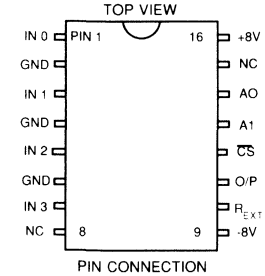


PIN CONNECTION
16 PIN SOIC

GX414,GX424



PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

GX434

Document No. 510 - 38 - 1

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	±13.5V *
Operating Temperature Range	0°C ≤ T_A ≤ 70° C
Storage Temperature Range	-65°C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	-4V ≤ V_{IN} ≤ +2.4V
Analog Input Current	50µA AVG, 10 mA peak
Logic Input Voltage	-4V ≤ V_L ≤ +5.5V **

* ±10V**, +5V, GX424 only

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX414CD	14 Pin DIP	0° to 70° C
GX414CK	16 Pin SOIC	0° to70° C
GX424CD	14 Pin DIP	0° to 70° C
GX424CK	16 Pin SOIC	0° to 70° C
GX434CD	14 Pin DIP	0° to 70° C
GX434CK	16 Pin SOIC	0° to 70° C

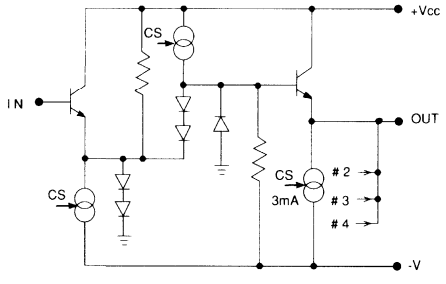


Fig.1 Crosspoint Equivalent Circuit

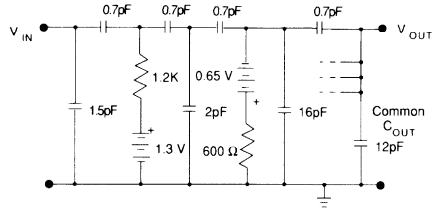


Fig. 2 Disabled Crosspoint Equivalent Circuit

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, C_L = 30 pF, R_L = 10kΩ unless otherwise shown.)

				GX414			GX424			GX434†			
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	±V_S		7	8	13.2	7	8	10	7	8	13.2	V
	Supply current	I+	Chip selected ($\overline{CS}$=0)	-	11	14	-	11	18	-	10.5	11.5	mA
			Chip not selected ($\overline{CS}$=1)	-	0.4	0.58	-	0.46	0.9	-	0.4	0.58	mA
		I-	Chip selected ($\overline{CS}$=0)	-	10.5	14	-	10.5	18	-	10.2	11.2	mA
			Chip not selected ($\overline{CS}$=1)	-	0.25	0.38	-	0.25	0.4	-	0.25	0.38	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs.	- -	+2 -1.2	- -	- -	+2 -1.2	- -	- -	+2 -1.2	-	V
	Analog Input Bias Current	I_{BIAS}		-	22		-	22	-	-	22	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25°C, 75 Ω resistor on each input to gnd	-2	5	12	-20	2	30	0	7	14	mV
	Output Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		-	+50	+200	-	+50	+300	-	+50	+200	µV/°C

† R_{EXT} = 33.2 kΩ, 1%

ELECTRICAL CHARACTERISTICS continued

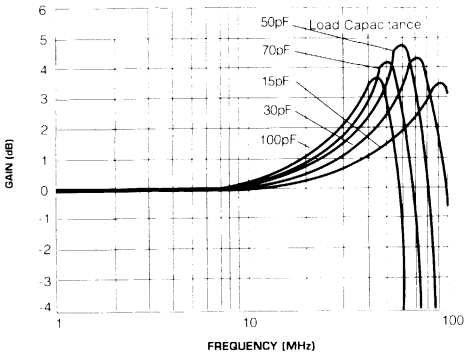
(V_S = ±8V DC, 0°C < T_A < 70°C, C_L = 30pF, R_L = 10kΩ unless otherwise shown)

				GX414			GX424			GX434*			
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
	Crosspoint Selection Turn-On Time	$t_{ADR\ ON}$	Control input to appearance of signal at the output	130	200	270	100	200	350	130	200	270	ns
	Crosspoint Selection Turn-Off Time	$t_{ADR\ OFF}$	Control input to disappearance of signal at output	390	600	800	300	600	950	390	600	800	ns
	Chip Selection Turn-On Time	$t_{CS\ ON}$	Control input to appearance of signal at output	200	300	400	150	300	450	200	300	400	ns
	Chip Selection Turn-Off Time	$t_{CS\ OFF}$	Control input to disappearance of signal at output	460	700	940	400	700	1100	460	700	940	ns
LOGIC	Logic Input Thresholds	V_{IH}	1	2.0	-	-	2.0	-	-	2.0	-	-	V
		V_{IL}	0	-	-	1.1	-	-	1.1	-	-	1.1	V
	Address Input Bias Current	$I_{BIAS(ADR)}$	Chip selected A0,A1 = 1	-	-	5.0	-	-	5.0	-	-	5.0	µA
			Chip selected A0,A1 = 0	-	-	0.1	-	-	0.1	-	-	0.1	nA
	Chip Select Bias Current	$I_{BIAS(CS)}$	$\overline{CS}$ = 1	-	-	1.0	-	-	1.0	-	-	1.0	nA
			$\overline{CS}$ = 0	-	-	30	-	-	30	-	-	30	µA
	Insertion Loss	I L	1V p-p sine or sq. wave at 100 kHz	0.02	0.03	0.05	0.015	0.03	0.06	0.025	0.03	0.04	dB
	Bandwidth (-3 dB)	B W		90	100	-	80	100	-	100	120	-	MHz
	Gain Spread at 8 MHz			-	-	±0.1	-	-	+0.46 -0.12	-	-	+0.06 -0.04	dB
	Input to Output Signal Delay Matching (chip to chip)	Δt_P	T_A = 25°C, R_S = 75Ω, f = 3.579545 MHz	-	-	±0.35	-	-	±0.8	-	-	±0.15	degrees
			0°C < T_A < 70°C, R_S as above, f as above	-	-	±0.7	-	-	±1.2	-	-	±0.3	degrees
	Input Resistance	R_N	Chip selected ($\overline{CS}$ = 0)	900	-	-	900	-	-	900	-	-	kΩ
DYNAMIC	Input Capacitance	C_{IN}	Chip selected ($\overline{CS}$ = 0)	-	2.0	-	-	2.0	-	-	2.0	-	pF
			Chip not selected ($\overline{CS}$ = 1)	-	2.4	-	-	2.4	-	-	2.4	-	pF
	Output Resistance	R_{OUT}	Chip selected ($\overline{CS}$ = 0)	-	14	-	-	14	-	-	14	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected ($\overline{CS}$ = 1)	-	15	-	-	15	-	-	15	-	pF
	Differential Gain	dg	at 3.579545 MHz	-	0.03	0.05	-	0.03	0.1	-	0.03	0.05	%
	Differential Phase	dp	V_{IN} = 40 IRE (Fig. 7)	-	0.012	0.025	-	0.012	0.05	-	0.012	0.025	degrees
	All Hostile Crosstalk (see graph)	$X_{TALK\ (AH)}$	Sweep on 3 inputs 1V p-p, 4th input has 10 Ω resistor to gnd, f = 5 MHz (Fig. 6)	94	97	-	92	97	-	94	97	-	dB
	Chip Disabled Crosstalk (see graph)	$X_{TALK(CD)}$	f = 10 MHz (Fig. 5)	100	110	-	90	110	-	100	110	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	84	120	-	60	120	-	360	450	-	V/µs
		-SR		70	100	-	50	100	-	160	200	-	V/µs

* R_{EXT} = 33.2kΩ 1%

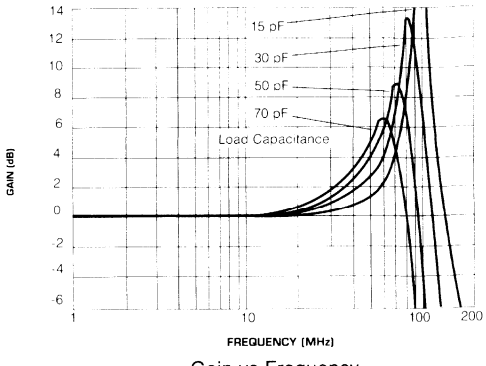
CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE DEVICES EXCEPT AT A STATIC-FREE WORKSTATION

GX414 GX424



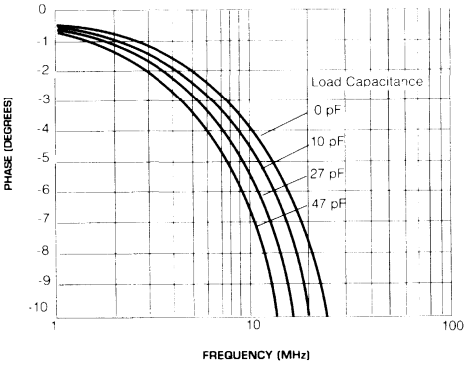
Gain vs Frequency

GX434



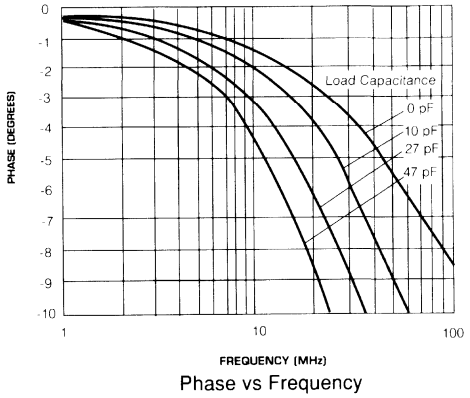
Gain vs Frequency

GX414 GX424



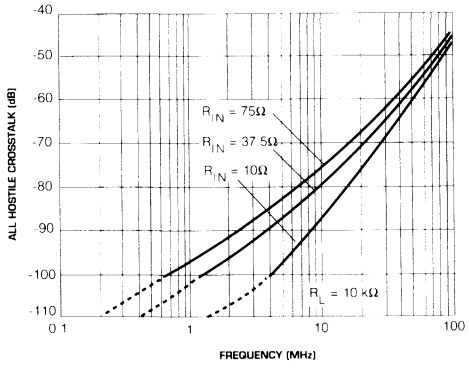
Phase vs Frequency

GX434



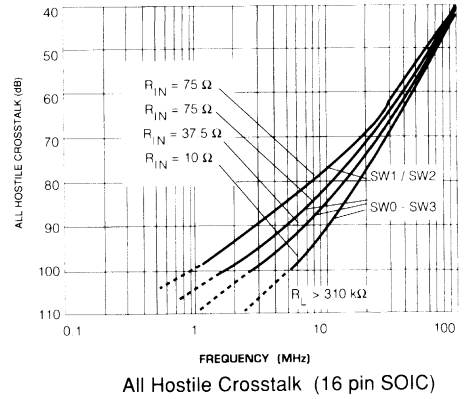
Phase vs Frequency

GX414 GX424 GX434



All Hostile Crosstalk vs Frequency (14 pin DIP)

GX414 GX424 GX434

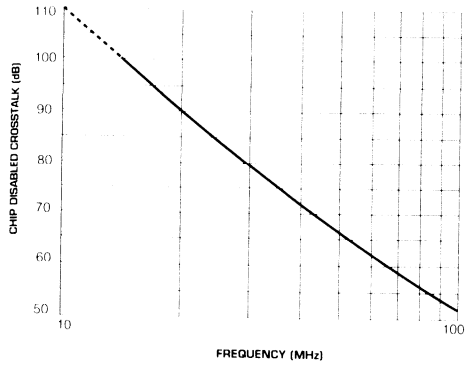


All Hostile Crosstalk (16 pin SOIC)

TYPICAL PERFORMANCE CURVES OF THE GX414, GX424 AND GX434

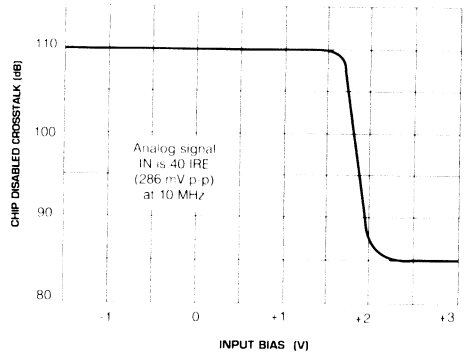
For all graphs, V_S = ±8 V DC and T_A = 25°C. The curves shown above represent typical batch sampled results.

GX414 GX424 GX434



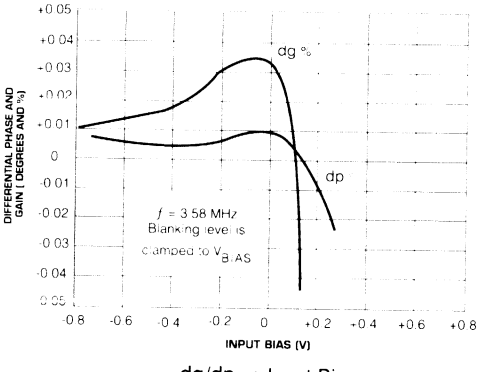
Chip Disabled Crosstalk vs Frequency

GX414 GX424 GX434



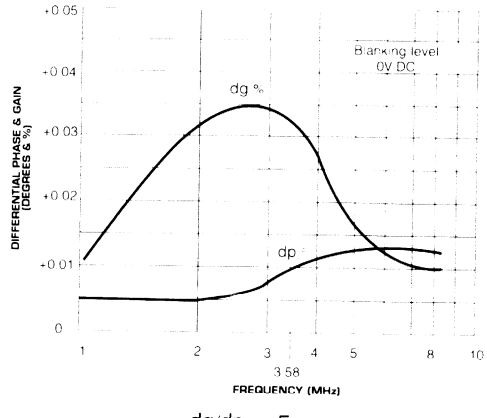
Chip Disabled Crosstalk vs Input Bias

GX414 GX424 GX434



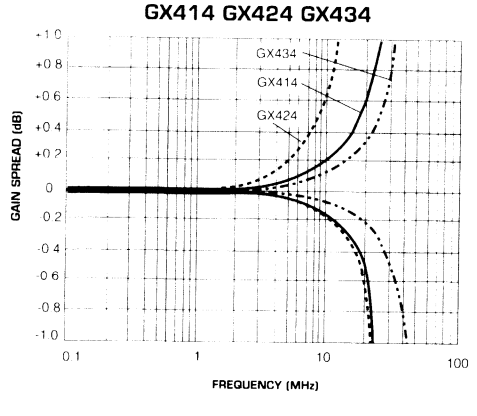
dg/dp vs Input Bias

GX414 GX424 GX434



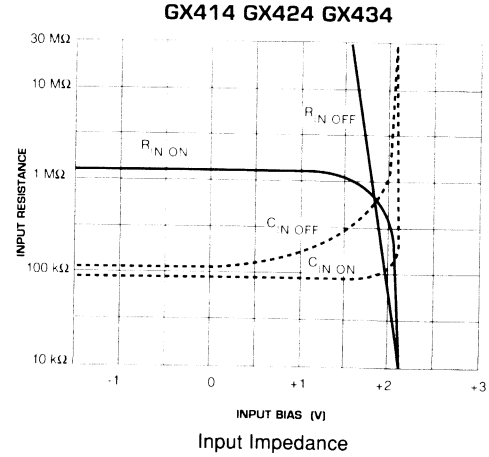
dg/dp vs Frequency

GX414 GX424 GX434



Normalized Gain Spread C_L = 30pF

GX414 GX424 GX434



Input Impedance

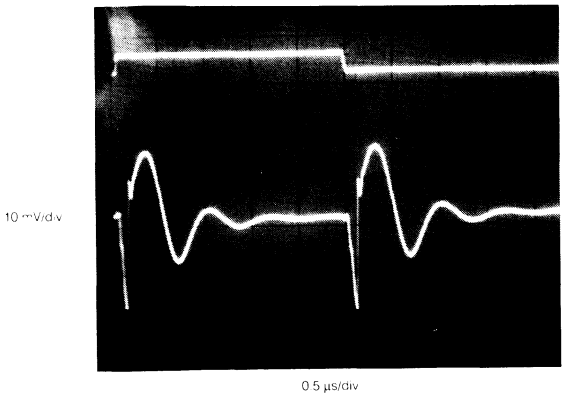


Fig.3 Switching Transient (crosspoint to crosspoint)

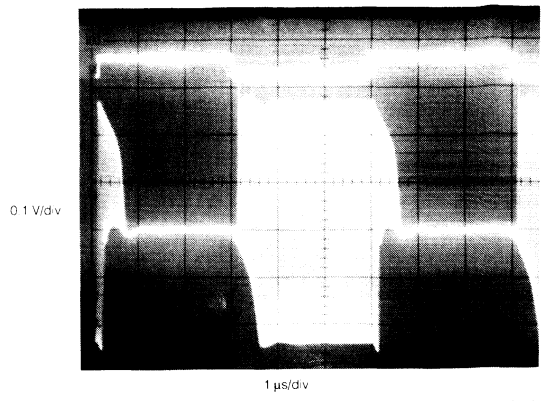


Fig. 4 Switching Envelope (crosspoint to crosspoint)

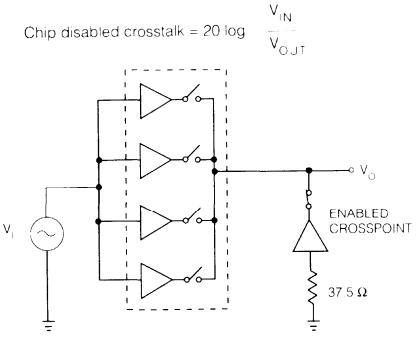


Fig. 5 Chip Disabled Crosstalk Test Circuit

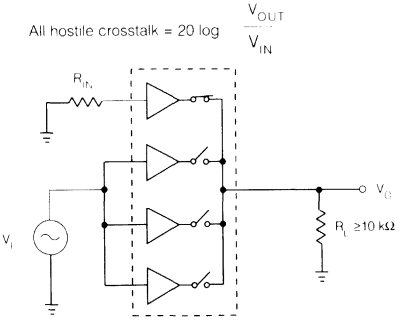


Fig. 6 All Hostile Crosstalk Test Circuit

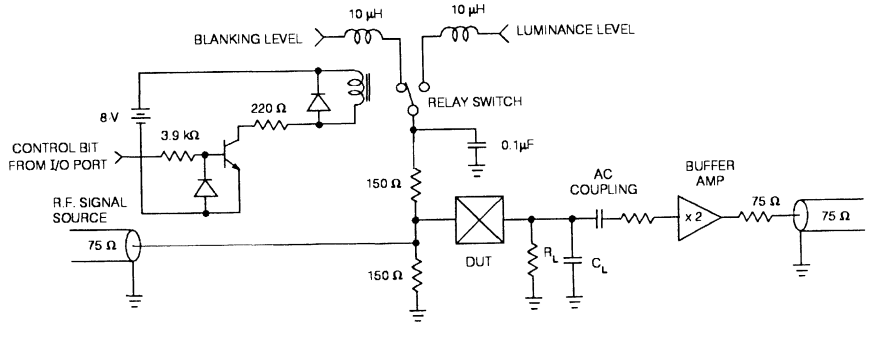


Fig. 7 Differential Phase and Gain Test Circuit

DIFFERENTIAL GAIN AND PHASE TEST CIRCUIT

The test circuit of Figure 7 allows two DC bias levels, set by the user, to be superimposed on a high frequency signal source. A computer controlled relay selects either the preset blanking or luminance level. One measurement is taken at each level and the change in gain or phase is calculated. This procedure is repeated one hundred times to provide a reasonably large sample.

The results are averaged to reduce the standard deviation and therefore improve the accuracy of the measurement.

The output from the device under test is AC coupled to a buffer amplifier which allows the buffer to operate at a constant luminance level so that it does not contribute any dg or dp to the measurement.

OPTIMISING THE PERFORMANCE OF THE GX414, GX424 AND GX434

1. Power Supply Considerations

Table 1 shows the effect on differential gain (dg) and differential phase (dp) of various power supply voltages that may be used. A nominal supply voltage of ±8 volts result in parameter values as shown in the top row of the table. By using other power supply voltage combinations, improvements to these parameters are possible at the sacrifice of increased chip power dissipation. Maximum degradation of the differential gain and phase occurs for the last combination of +12 , -5 volts along with an increase in power dissipation; these voltages are not recommended.

Supply Voltage	Differential Gain % (Typical)	Differential Phase degrees (Typical)
±8	0.030	0.012
+8/ -12	0.010	0.007
±12	0.010	0.007
+12/ -5	0.084	0.080

Table 2 shows the general characteristic variations of the GX4 family when different combinations of power supply voltages are used. These changes are relative to a circuit using ± 8 volts Vcc.

Supply Voltage	Characteristic Changes
± 5	- lower logic thresholds - max logic I/P (≈ 4.5V) - loss of off isolation (≈20 dB) - poorer dg and dp
+8/ -12	- slight increase in negative supply current - slight decrease in offset - very similar frequency response - better dg and dp
±12	- increase in supply current (10%) - increase in offset (≈ 2-4 mV) - very similar frequency response - better dg and dp
+12/ -5	- loss in off isolation (≈20 dB) - poorer dg and dp

These devices do not require input DC biasing to optimise dg or dp nor do they need switching transient suppression at the output. Furthermore, both the analog signal and logic circuits within the chip use one common power supply, making power supply configurations relatively simple and straightforward. Several of the input characteristic graphs on pages 4-5 show that for best operation, the input bias should be 0 volts. The switching transient photographs on page 6 show how small the actual transients are and clearly show the make-before-break action of the GX4 family of video crosspoint switches.

2. Frequency Response Considerations

At frequencies higher than 1 MHz, the output impedance of the crosspoint switches can be modelled as a voltage generator having a series resistance and a series inductance. The gain/ frequency characteristics exhibit peaking above 10 MHz due to the internal equivalent series inductance combined with any load capacitance. The peaking can be reduced by adding external series resistance to the output of the crosspoint. Figure 8 shows the effect of adding a 33Ω resistor to the output of a circuit having 47 pF effective load capacitance. This amount of load capacitance represents the equivalent of a 16 x1 crosspoint configuration using four ICs. Even though the frequency response has been flattened, the differential phase and gain have now changed as shown in Figure 9.

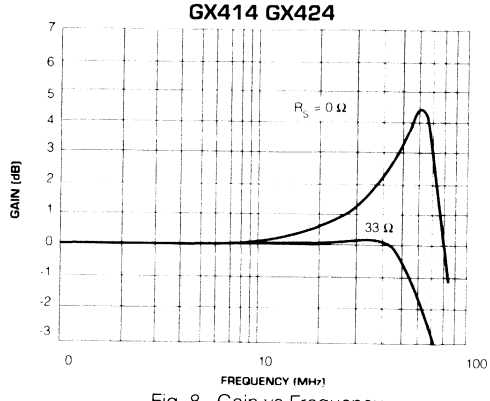


Fig. 8 Gain vs Frequency

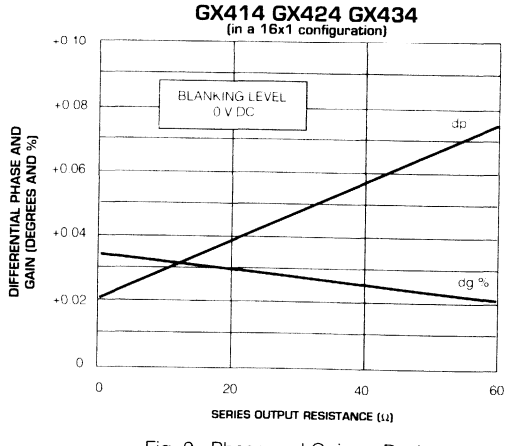


Fig. 9 Phase and Gain vs Resistance

The internal circuitry of the GX434 has been modified slightly in order to widen the bandwidth. This results in more peaking but the peaking frequency is higher. The response can be flattened by using an external series resistor. Test results yield a value of approximately 38Ω for a 16 x 1 configuration.

3. Load Resistance Considerations

This family of crosspoint switches are optimised for load resistances equal to or greater than 3 kΩ. Figure 10 shows the effect on the differential gain and phase when the load resistance is varied from 100 Ω to 100 kΩ.

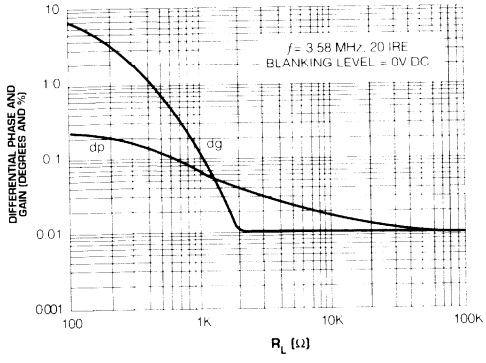


Fig. 10 dg/dp vs R_L

The negative slew rate is dependant upon the output current and load capacitance as shown below.

$$-SR = \frac{I + 3\ mA}{C_L} \qquad I \leq 8\ mA$$

The current I is determined from the following equation:

$$I = \frac{-V_{EE}}{R} \qquad R \geq 1\ k\Omega$$

It is possible to increase the negative slew rate (-S.R.) and thus the large signal bandwidth, by adding a resistance from the output to - V_{EE}. This resistor increases the output current above the 3 mA provided by the internal current generator and increases the negative slew rate. The additional slew rate improving resistance must not be less than 1kΩ in order to prevent excessive currents in the output of the device. An adverse effect of utilising this negative slew rate improving resistor, is the increase in differential phase from typically 0.009° to 0.014°. Under these same conditions, the differential gain drops from typically 0.033 % to 0.021 %.

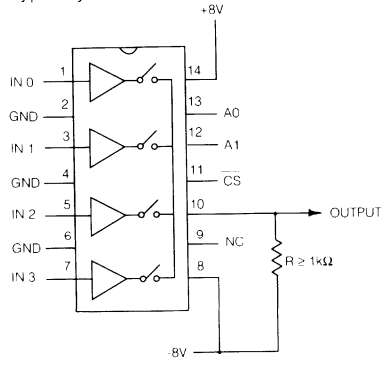


Fig.11 Negative Slew Rate (-SR) Improvement

4. Multi-chip Considerations

Whenever multi-chip bus systems are to be used, the total input and output capacitance must be carefully considered. The input capacitance of an enabled crosspoint (chip selected), is typically only 2 pF and increases slightly to 2.4 pF when the chip is disabled. The total output capacitance when the chip is disabled is approximately 15 pF per chip.

Usually the GX4 crosspoint switches are used in a matrix configuration of (n x 1) crosspoints perhaps combined in an (n x m) total routing matrix. This means for example, that four ICs produce a 16 x 1 configuration and have a total output capacitance of 4 x15 pF or 60 pF if all four chips are disabled. For any one enabled crosspoint, the effective load capacitance will be 3 x15 pF or 45 pF.

In a multi-input/multi-output matrix, it is important to consider the total input bus capacitance. The higher the bus capacitance and the more it varies from the ON to OFF condition, the more difficult it is to maintain a wide frequency response and constant drive from the input buffer. A 16 x 16 matrix using 64 ICs (16 x 4), would have a total input bus capacitance of 16 x 2.4 pF or 40 pF.

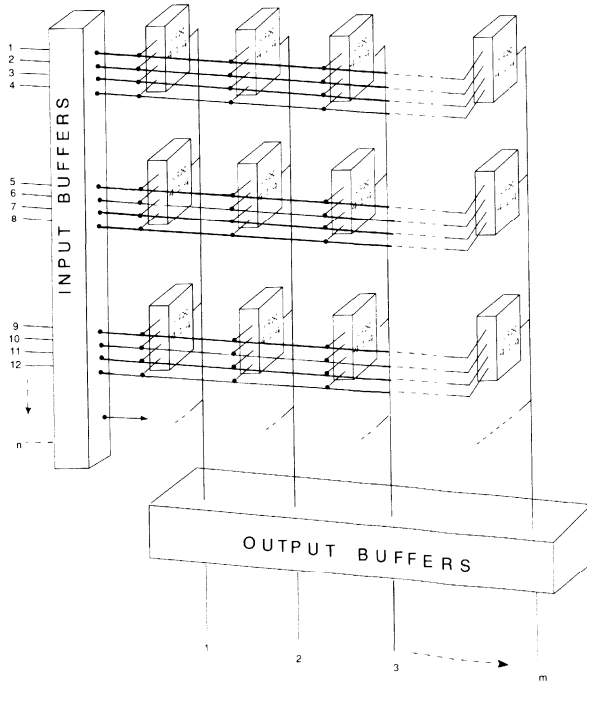


Fig.12 Multi-chip Connections

APPLICATIONS INFORMATION

The GX4 family of video switches are very high performance, wideband circuits requiring careful external circuit design. Good power supply regulation and decoupling are necessary to achieve optimum results. The circuit designer must use proper lead dress, component placement and PCB layout as in any high frequency circuit.

Functionally, the video switches are non-inverting, unity gain bipolar switches with buffered inputs requiring DC coupling and 75Ω line terminating resistors when directly driven from 75Ω cable. The output must be buffered to drive 75Ω lines. This is usually accomplished with the addition of an operational amplifier/ buffer which also allows adjustments to be made to the gain, offset and frequency response of the overall circuit. A typical video routing application is shown in Figure 13. Four ICs are used in a 16 x 1 crosspoint switching circuit.

An external address decoder is shown which generates the 16 address and chip enable codes from a binary number. The address inputs to each chip are active high while the chip select inputs are active low. Depending on the application and speed of the logic family used, latches may be required for synchronization where timing and delays are critical. Since the individual crosspoint switching circuits are unidirectional bipolar elements, low crosstalk and high isolation are inherent. The make-before-break switching characteristics of the GX414 means virtually 'glitch' free switching.

AVAILABLE PACKAGING
14 pin DIP and 16 pin SOIC

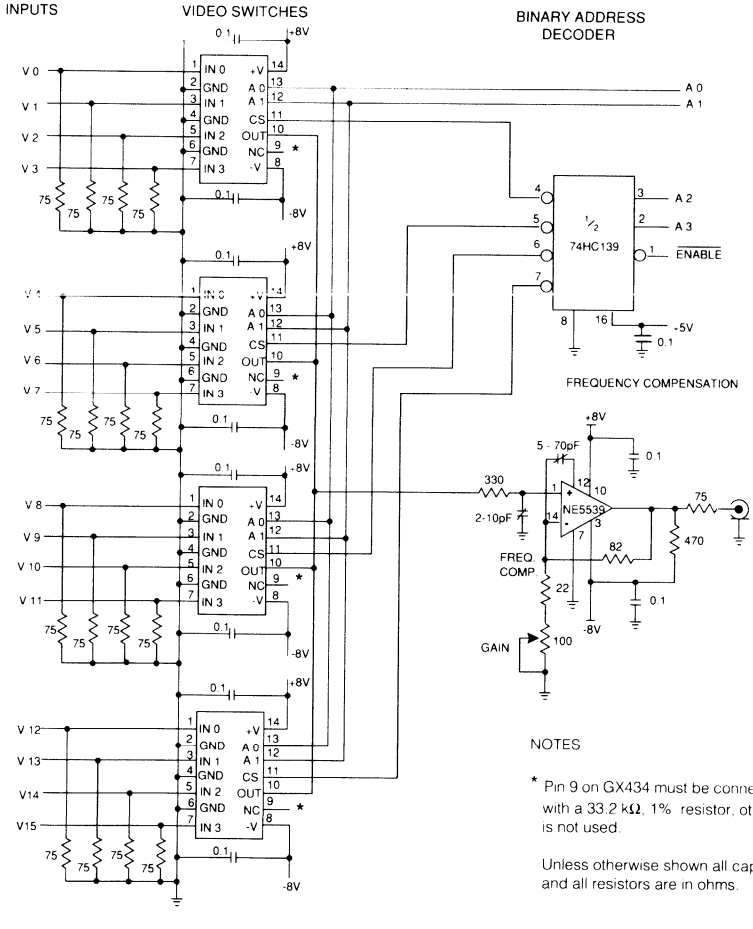


Fig.13 16 x 1 Video Crosspoint Circuit

GENNUM CORPORATION

Monolithic 4x1 Video Crosspoint Switch

GX414A PRELIMINARY DATA SHEET

FEATURES

* low disabled power consumption: 5.2 mW
* low differential gain: 0.03% typ. at 4.43 MHz
* low differential phase: 0.012° typ. at 4.43 MHz
* bandwidth (-3dB) 100 MHz with 30 pF load
* all hostile crosstalk at 5 MHz -97dB typ.
* low insertion loss 0.05 dB max at 100 kHz
* off isolation 110 dB at 10 MHz
* fast make before break switching: 200 ns typ.
* TTL and 5 volt CMOS compatible logic inputs
* for NTSC, PAL and SECAM applications
* low cost 14 pin DIP and16 pin SOIC packages

CIRCUIT DESCRIPTION

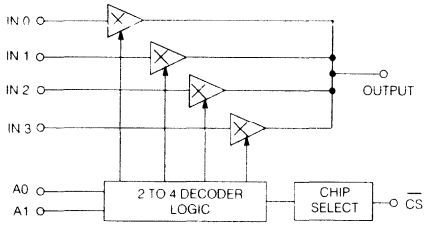
The GX414A is high performance low cost monolithic 4x1 video crosspoint switch incorporating four analog video switches and a 2 to 4 address decoder. An enabled input allows paralleled GX414As to be operated in a switching matrix with multiple inputs and a common output. Unlike similar devices using MOS bilateral switching elements, the GX414A represents a fully buffered unilateral transmission path when enabled. The GX414A requires ±8V and is designed for use in video switching applications. Logic inputs are TTL and 5V CMOS compatible, providing input select and output enable functions.

APPLICATIONS

Glitch free analog switching for...

* High quality video routing
* A/D input multiplexing
* Sample and hold circuits
* TV/ CATV/ monitor switching
* Instrumentation and communication equipment

FUNCTIONAL SCHEMATIC

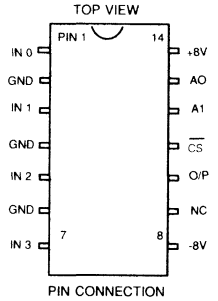


TRUTH TABLE

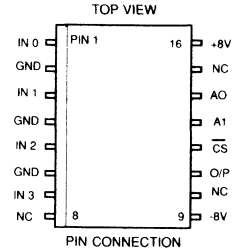
CS	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION



PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX414ACD	14 Pin DIP	0° to 70° C
GX414ACK	16 Pin SOIC	0° to 70° C

Document No. 510-19-1

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5V
Operating Temperature Range	$0°C \leq T_A \leq 70° C$
Storage Temperature Range	$-65°C \leq T_S \leq 150° C$
Lead Temperature (Soldering, 10 Sec)	260° C

Parameter	Value
Analog Input Voltage	$-4V \leq V_{IN} \leq +2.4V$
Analog Input Current	50µA AVG, 10 mA peak
Logic Input Voltage	$-4V \leq V_L \leq +5.5V$

ELECTRICAL CHARACTERISTICS ($V_S = \pm 8V$ DC, $0°C < T_A < 70°C$, $R_L = 10K$, $C_L = 30$ pF, unless otherwise shown.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	$\overline{CS} = 0$ V+		-	11	14	mA
	V-		-	10.5	14	
	$\overline{CS} = 1$ V+		-	0.4	0.58	
	V-		-	0.25	0.38	
Analog Output Voltage Swing	Extremes before clipping occurs		-	+2.0	-	V
			-	-1.2	-	
Output Offset voltage	75Ω on each input ground		-2	5	12	mV
Output Offset Drift	$\Delta V_{OSC} / \Delta T$		-	+50	+200	µV / °C
Address Logic Delay	Control input to appearance of signal on output		130	200	270	ns
Chip Selection Delay	Control input to appearance of signal on output		200	300	400	ns
Logic Input Threshold	1		-	-	1.1	V
	0		2	-	-	V
Logic Input Current	A0, A1 = 1		-	-	5.0	µA
	A0, A1 = 0		-	-	0.1	nA
	$\overline{CS} = 1$		-	-	1.0	nA
	$\overline{CS} = 0$		-	-	30.0	µA
Insertion Loss	1V p-p sine or sq.wave at 100 kHz		0.02	0.03	0.05	dB
Gain Spread at 8 MHz			-	-	±0.25	dB
Bandwidth (-3dB)			90	100	-	MHz
Differential Gain	at 3.58 or 4.43 MHz		-	0.03	0.05	%
Differential Phase	at 3.58 or 4.43 MHz		-	0.012	0.025	degrees
Input to Output Delay Matching (chip-chip)	75Ω source impedance at 3.579545 MHz	$T_A = 25°$	-	-	±0.6	degrees
		Full temp.	-	-	±1.0	degrees
All Hostile Crosstalk	Sweep on 3 inputs 1V p-p 4th input 10 Ω to gnd at 5 MHz		94	97	-	dB
Chip Disabled Crosstalk	14Ω on output to gnd at 10 MHz		100	110	-	dB
Input Resistance	$\overline{CS} = 0$		-	960	-	kΩ
Input Capacitance	$\overline{CS} = 0$		-	2.0	-	pF
	$\overline{CS} = 1$		-	2.4	-	pF
Output Resistance	$\overline{CS} = 0$		-	14	-	Ω
Output Capacitance	$\overline{CS} = 1$		-	15	-	pF
Slew Rate		+SR	-	40	-	V/µs
	V_{IN} = 3V p-p (C_L = 0 pF)	-SR	-	40	-	V/µs

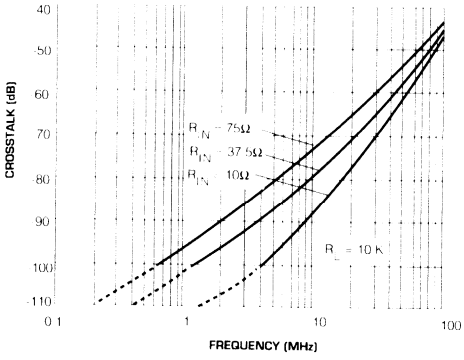


Fig. 1 Typical All Hostile Crosstalk Performance (14 pin DIP)

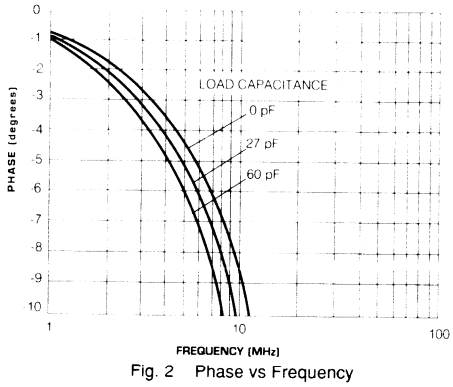


Fig. 2 Phase vs Frequency

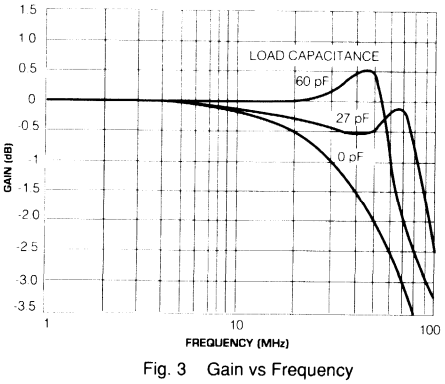


Fig. 3 Gain vs Frequency

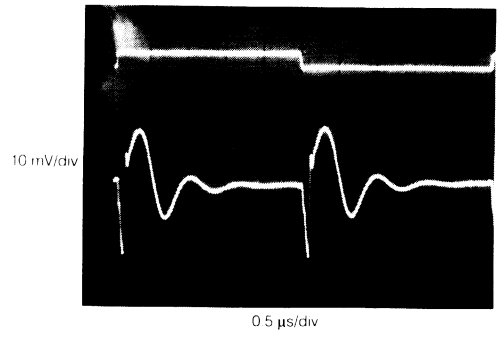


Fig. 4 Switching Transient (crosspoint-to-crosspoint)

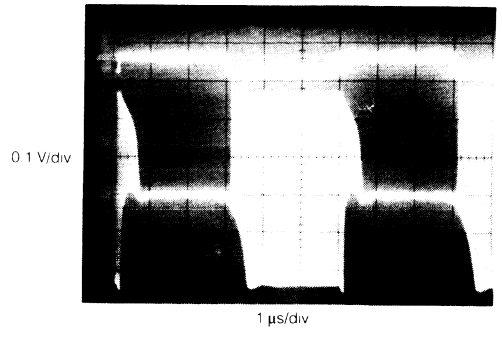


Fig. 5 Switching Envelope (crosspoint-to-crosspoint)

APPLICATION INFORMATION

As expected with any wide bandwidth circuit, the layout is critical. Good power supply regulation and bypassing are necessary, along with good high frequency design practice. Proper lead dress, component placement and PC board layout must be exercised for optimum performance.

The GX414A is non-inverting. Frequency peaking is compensated on-chip and optimised for a 60 pF load. The inputs are buffered and require 75Ω line terminating resistors when driven from 75Ω cable. The output must be buffered to drive 75Ω lines. The addition of an amplifier/buffer also allows adjustments to be made to the gain, offset and frequency response of the circuit. By reducing the load capacitance from 60 pF, the GX414A can be used to compensate for the frequency peaking of the buffer.

A typical application is shown in Figure 6 on the next page . Two GX414A devices are paralleled to form an 8x1 crosspoint switch. The three address lines make use of the A0, A1 and $\overline{CS}$ inputs. If more than two devices are used in parallel, a decoder will be necessary to generate the extra address inputs. Depending on the application and the speed of the logic family employed, latches may be required for synchronization where timing and delays are important.

The active switching circuitry of the GX414A will ensure low crosstalk and high performance over an input voltage range of -1.2 V to +2.0 V.

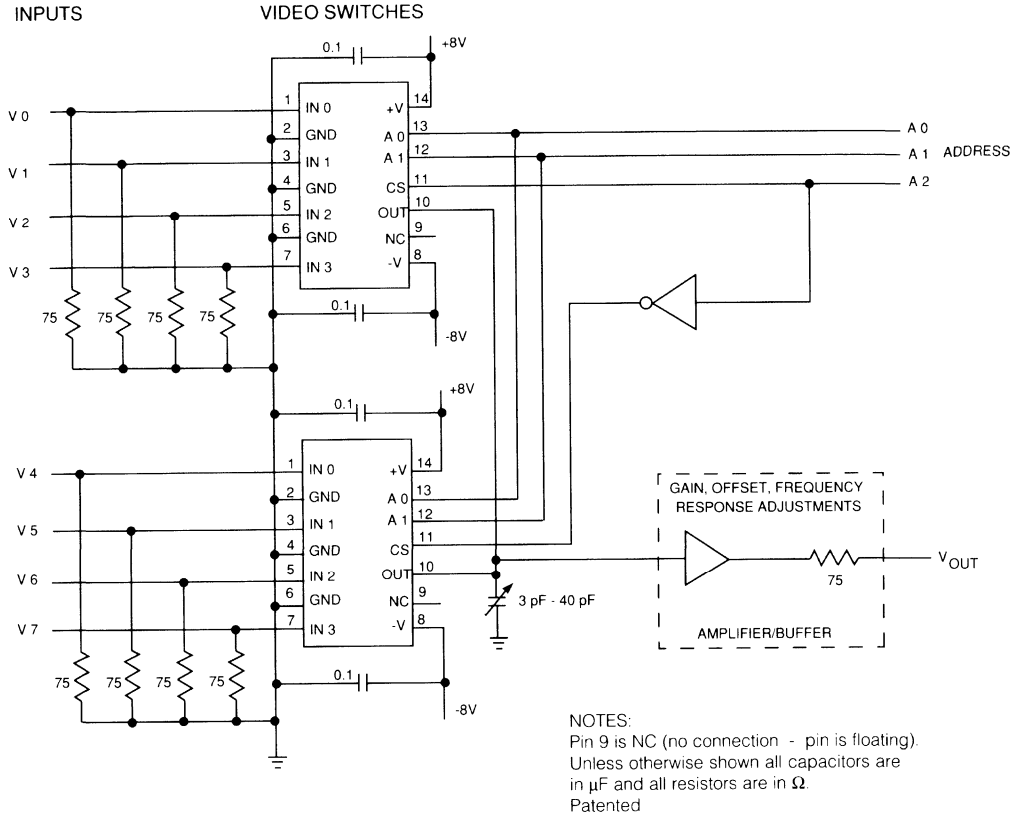


Fig. 6 Video Multiplexer Incorporating Two GX414As

AVAILABLE PACKAGING

14 and 16 pin Molded DIP

GENNUM CORPORATION

Monolithic 4x1 Video Crosspoint Switch

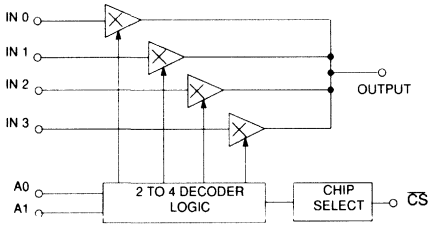
GX214 PRELIMINARY DATA SHEET

VBD 6

FEATURES

* low cost
* differential gain at 3.58 MHz, 0.05% max.
* differential phase at 3.58 MHz, 0.05 deg. max.
* off isolation better than 90 dB at 10 MHz
* all hostile crosstalk at 3.58 MHz, 75 dB typ. (R_{IN}= 75 Ω)
* make-before-break switching

FUNCTIONAL BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The GX214 is a low cost 4x1 video crosspoint switch containing four analog video switches and a 2 to 4 decoder. A Chip Select input allows paralleled GX214s to be operated in a switching matrix.

The GX214 represents a fully buffered, unilateral transmission path when enabled. When disabled, the output is high impedance.

The device operates from ±7.5 V to ±9.5 V supplies with TTL and 5 V CMOS compatible input logic levels.

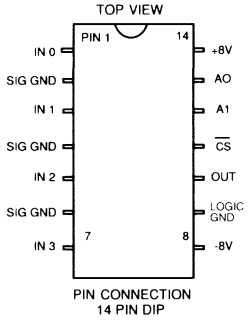
APPLICATIONS

* CATV and CCTV systems
* low cost video routing

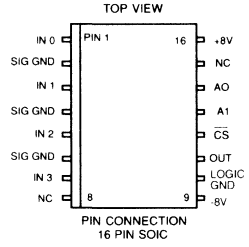
TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE



PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX214CD	14 Pin DIP	0° to 70°C
GX214CK	16 Pin SOIC	0° to 70°C

AVAILABLE PACKAGING

14 pin DIP and 16 pin SOIC

CAUTION
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ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±10.0 V
Operating Temperature Range	0 °C ≤ T_A ≤ 50 °C
Storage Temperature Range	-65 °C ≤ T_S ≤ 150 °C

Parameter	Value
Lead Temperature (Soldering, 10 Sec)	260 °C
Analog Input Voltage	-4 V ≤ V_{IN} ≤ V_{CC}+0.3 V
Logic Input Voltage	0 V ≤ V_L ≤ 5.5 V

NOTE: A short from output to ground or either supply will destroy the device. For R_{EXT} use a 1.2 kΩ 1%, $^1/_4$ W resistor.

ELECTRICAL CHARACTERISTICS (V_S = ±8 V DC, 0°C < T_A < 70 °C, R_L = 1.21 kΩ to V_{EE}, C_L = 30pF)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	$\pm V_S$		7.5	8.0	9.5	V
	Supply Current	I+	Chip selected ($\overline{CS}$=0)	-	14	20	mA
			Chip not selected ($\overline{CS}$=1)	-	0.6	0.95	mA
		I-	Chip selected ($\overline{CS}$=0)	-	13	18	mA
			Chip not selected ($\overline{CS}$=1)	-	0.58	0.88	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-	-	+5.0 -1.2	V
	Analog Input Bias Current	I_{IN}		-	25	-	µA
	Output Offset Voltage	V_{OS}	75Ω resistor on each input to ground	-45	-80	-120	mV
LOGIC	Turn-On Time	t_{ON}	Control input to disappearance of signal at output.	700	900	1100	ns
	Turn-Off Time	t_{OFF}	Control input to disappearance of signal at output.	1.2	2.0	3.0	µs
	Logic Input Thresholds	V_{IH}	1	2.4	-	-	V
		V_{IL}	0	-	-	0.6	V
	Logic Input Bias Current	I_{BIAS}	Chip Selected A0,A1 = 1	-	-	10	nA
			Chip Selected A0,A1 = 0	-	-	60	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.1	0.13	0.16	dB
	Bandwidth (-3dB)	B.W.		65	85	-	MHz
	Input Resistance	R_{IN}	Chip selected ($\overline{CS}$ = 0)	900	-	-	kΩ
	Input Capacitance	C_{IN}	Chip selected ($\overline{CS}$ = 0)	-	2.2	-	pF
			Chip not selected ($\overline{CS}$=1)	-	2.0	-	pF
	Output Resistance	R_{OUT}	Chip selected ($\overline{CS}$=0)	-	9	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected ($\overline{CS}$=1)	-	12	-	pF
	Differential Gain	dg	at 3.58 MHz	-	-	0.05	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	-	0.05	deg.
	All Hostile Crosstalk	$X_{TALK(AH)}$	Sweep on 3 inputs 1V p-p 4th input has 75 Ω resistor to gnd. f = 10 MHz	73	75	-	dB
	Chip Disabled Crosstalk	$X_{TALK(CD)}$	One xpt on output to ground f = 10 MHz	90	100	-	dB

APPLICATION INFORMATION

The circuit layout of any wideband circuit is critical. Good high frequency design practice, proper lead dress and PCB component placement along with a well regulated and decoupled power supply will assure optimum performance of the crosspoint.

The GX214 is non-inverting. The inputs are buffered and require 75Ω line terminating resistors when driven from 75Ω cable. The inputs may be driven directly from an amplifier which has low output impedance.

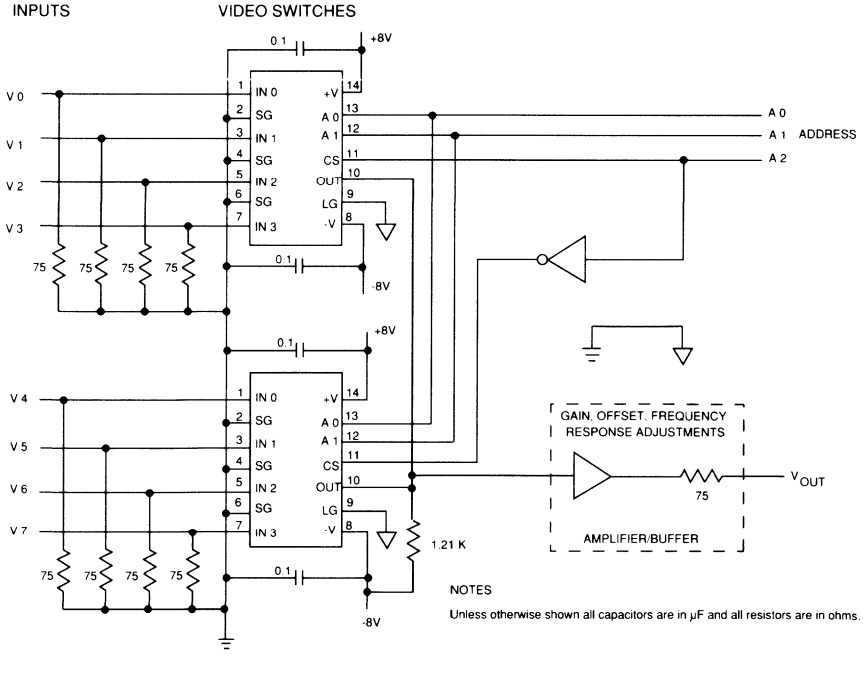
The output of the GX214 must be buffered to drive 75 Ω lines. The addition of an amplifier/buffer also allows adjustments to be made to the gain, offset and frequency response of the circuit.

Signal Ground (SG) pins 2, 4 and 6 must be joined together and preferably form part of a ground plane. The Signal Ground must also be connected to the ±8 V power supply ground. The potential of the Logic Ground (LG) pin 9 can deviate from the Signal Ground by ±0.5 V maximum. Alternatively, the signal and logic grounds can be joined together at one point only.

An external load current of 2 to 8 mA should be supplied from each output bus to negative supply. For most applications a load resistor of 1.21 kΩ, 1% is recommended to minimize offset drift with temperature. In order to improve differential phase and tighten the insertion loss tolerance, an external constant current active load may be substituted for the load resistor. Note however, that since only one GX214 output drives the output bus at any one time, only one external load is needed for the bus.

A typical application is shown below. Two GX214 ICs are paralleled to form an 8x1 crosspoint matrix. The three address lines make use of the A0, A1 and $\overline{CS}$ inputs. If more than two devices are used in parallel, a decoder is necessary in order to generate the extra address inputs.

Depending on the application and the speed of the logic family used, latches may be required for synchronization where timing delays are critical. The active switching circuitry of the GX214 ensures low crosstalk and high performance over an input voltage range of -1.2 to +5.0 volts.



8x1 Video Multiplexer Incorporating Two GX214 Devices

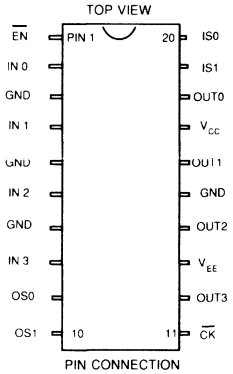
Monolithic 4x4 Video Crosspoint Matrix

GX244 ADVANCE INFORMATION SHEET

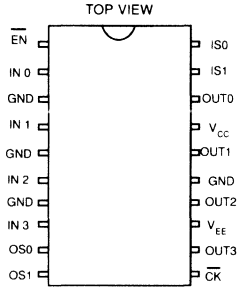
FEATURES

* low cost
* maximum packing density
* 16 crosspoints in a 20 pin DIP or SOIC package
* fully buffered unilateral signal path
* low crosstalk
* wide bandwidth
* microprocessor-compatible control interface
* TTL and 5 V CMOS logic inputs
* ±4.5 V to ±13.2 V supplies

PIN CONFIGURATIONS



PIN CONNECTION
20 PIN PLASTIC DIP



PIN CONNECTION
20 PIN PLASTIC SOIC
(300 mil body)

CIRCUIT DESCRIPTION

The GX244 is a microprocessor-compatible 4x4 video crosspoint matrix implemented in bipolar monolithic technology. The device maximizes crosspoint density by integrating 16 crosspoints in a 20 pin DIP or SOIC package.

The GX244 offers improvements over CMOS switches, delivering wider bandwidth, lower crosstalk and lower distortion, for upgraded performance in industrial video applications.

For use in NxM routing matrices, the device features high, nearly constant input impedance, coupled with high output impedance in the disabled state. This allows multiple devices to be paralleled at the inputs and outputs without additional circuitry. A fully buffered unilateral signal path ensures very low output-to-input feedback while generating minimal output switching transients through make-before-break switching.

The six logic inputs of the GX244 allow four crosspoints to be on at once. The input select (IS0, IS1) and enable ($\overline{EN}$) pins are decoded to determine which one of the four inputs will be selected. This data is clocked into one of the four control latches as determined by the output select (OS0, OS1) pins. A low state on the clock input ($\overline{CK}$) causes the selected control latch to become transparent; data is latched as the clock returns high. Using this method, one output bus can be switched at a time.

APPLICATIONS

* closed-circuit TV switchers
* security / surveillance systems
* machine vision systems
* cable TV / industrial video

TRUTH TABLES

Input Control

$\overline{EN}$	IS0	IS1	INPUT SELECTED	OUTPUT SIGNAL
0	0	0	0	IN 0
0	0	1	1	IN1
0	1	0	2	IN2
0	1	1	3	IN3
1	X	X	none	HI-Z

Output Control

$\overline{CK}$	OS0	OS1	OUTPUT ADDRESSED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
↓	X	X	NCHG
1	X	X	NCHG

X	don't care - immaterial
NCHG	no change - matrix maintains previous state
↓	rising clock edge
none	no input is selected

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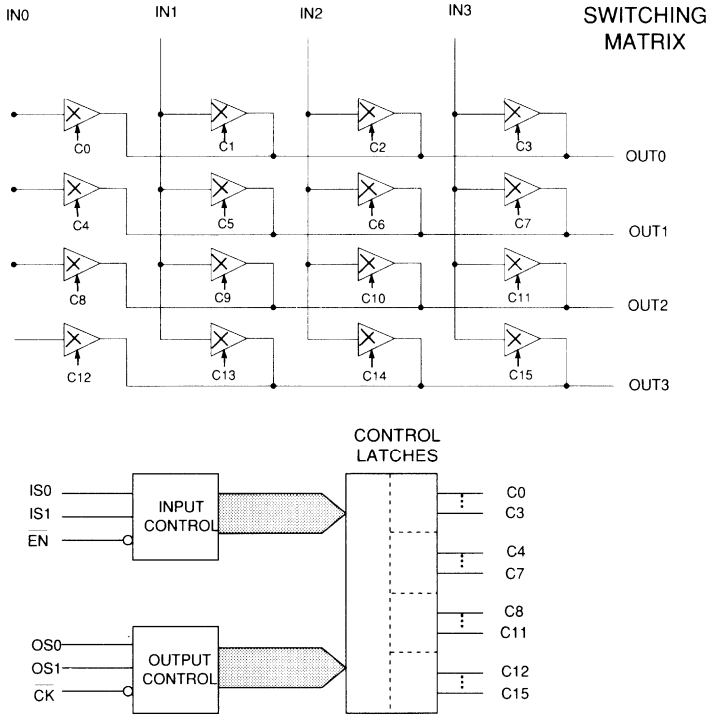


FUNCTIONAL BLOCK DIAGRAM

Monolithic 5x1 Video Crosspoint Switch

GX415 ADVANCE INFORMATION NOTE

VBD 8

FEATURES

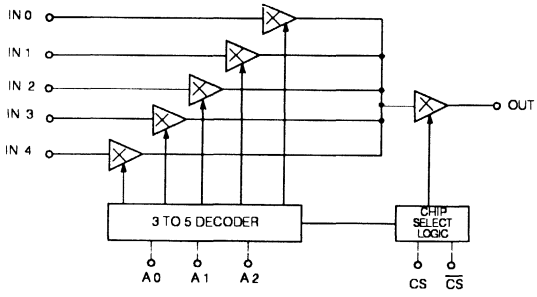
* low differential phase and gain
* make-before-break switching
* TTL and 5 V CMOS compatible logic levels
* 18 pin DIP packaging

CIRCUIT DESCRIPTION

The GX415 is a bipolar monolithic 5x1 crosspoint switch suited to decade multiplexing systems.

The bipolar signal path is characterized by low differential phase and gain. A fully buffered and unilateral circuit assures high off isolation and low crosstalk.

FUNCTIONAL BLOCK DIAGRAM



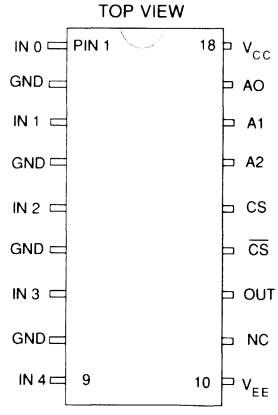
APPLICATIONS

*broadcast quality routing
*CCTV/CATV/monitor switching
*decade multiplexing

TRUTH TABLE

CS	$\overline{CS}$	A2	A1	A0	OUT
0	X	X	X	X	HI-Z
X	1	X	X	X	HI-Z
1	0	0	0	0	IN 0
1	0	0	0	1	IN 1
1	0	0	1	0	IN 2
1	0	0	1	1	IN 3
1	0	1	0	0	IN 4

X = don't care



PIN CONNECTION
18 PIN DIP

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GENNUM CORPORATION

Monolithic 8x1 Video Crosspoint Switch

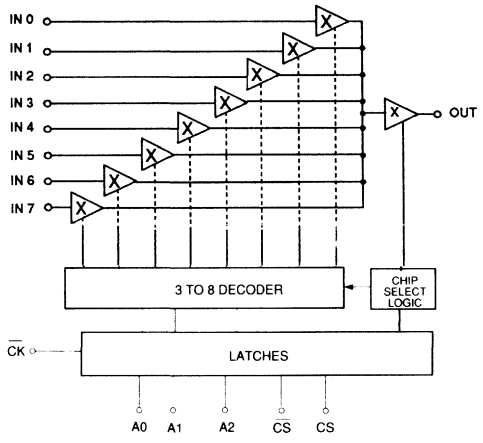
GX418 TENTATIVE DATA SHEET

VBD 9

FEATURES

* low differential phase and gain
* low crosstalk and high off-isolation
* TTL and 5V CMOS compatible logic input levels
* fully buffered unilateral signal path
* minimal switching transients
* 28 pin PLCC packaging
* simplified microprocessor interface
* true and inverse chip select allows for paralleled operation

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

A2	A1	A0	CS	$\overline{CS}$	$\overline{CK}$	OUT
X	X	X	0	X	0	HI-Z
X	X	X	X	1	0	HI-Z
0	0	0	1	0	0	IN 0
0	0	1	1	0	0	IN 1
0	1	0	1	0	0	IN 2
0	1	1	1	0	0	IN 3
1	0	0	1	0	0	IN 4
1	0	1	1	0	0	IN 5
1	1	0	1	0	0	IN 6
1	1	1	1	0	0	IN 7
X	X	X	X	X	↑	multiplexer maintains previous state
X	X	X	X	X	1	

X = don't care.

CIRCUIT DESCRIPTION

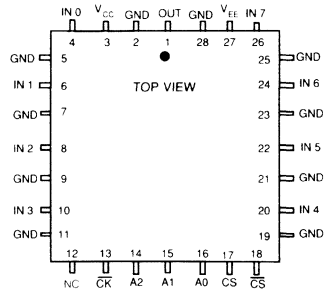
The GX418 is a microprocessor-compatible 8x1 video multiplexer featuring broadcast quality specifications, implemented in bipolar monolithic technology.

For use in NxM routing matrices, this device features very high, nearly constant input impedance, coupled with very high output impedance in the disabled state. This allows multiple devices to be paralleled at the inputs and output without additional circuitry. A fully buffered unilateral signal path ensures negligible output to input feedback while delivering minimal output switching transients through make-before-break switching.

The GX418 provides complementary chip select inputs to allow easy expansion into Nx1 configurations. The device operates over a supply voltage range from ±4.5 to ±13.2 volts.

APPLICATIONS

* high density video routing switchers
* video production and master control switchers
* CCTV/CATV
* PCM/data routing matrices



PIN CONNECTIONS
28 PIN PLCC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5 V
Operating Temperature Range	0° C ≤ T_A ≤ 70° C
Storage Temperature Range	-65° C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec.)	260° C
Analog Input Voltage	-4V ≤ V_{IN} ≤ 6V or V_{CC}+0.3 V
Logic Input Voltage	0 V ≤ V_L ≤ 5.5 V

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ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, R_L = 10kΩ, C_L = 30pF)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	Supply Voltage	$\pm V_S$		4.5	-	13.2	V
DC SUPPLY	Supply Current	I+	Chip selected ($\overline{CS}$=0)	-	12	-	mA
			Chip not selected ($\overline{CS}$=1)	-	1.4	-	mA
		I-	Chip selected ($\overline{CS}$=0)	-	11	-	mA
			Chip not selected ($\overline{CS}$=1)	-	0.23	-	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-1.8	-	6	V
	Output Offset Voltage	V_{OS}	T_A = 25°C, 75Ω resistor on each input to gnd	-12	0	12	mV
LOGIC	Crosspoint Turn-On Time	t_{ON}	Control input to appearance of signal at output.	-	500	-	ns
	Crosspoint Turn-Off Time	t_{OFF}	Control input to disappearance of signal at output.	-	750	-	ns
	Minimum clock pulse width	t_{PW}	Control input to disappear ance of signal at output.	200	-	-	ns
	Logic Input	V_{IH}	1	2.0	-	-	V
	Thresholds	V_{IL}	0	-	-	1.1	V
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.04	0.055	0.09	dB
	Bandwidth (-3dB)	B.W.		90	-	-	MHz
	Gain spread at 8 MHz			-	-	±0.06	dB
	Input Resistance	R_{IN}	Chip selected ($\overline{CS}$=0)	1	-	-	MΩ
	Input Capacitance	C_{IN}	Chip selected (CS=0)	-	2.0	-	pF
			Chip not selected ($\overline{CS}$=1)	-	2.2	-	pF
	Output Resistance	R_{OUT}	Chip selected ($\overline{CS}$=0)	-	14	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected ($\overline{CS}$=1)	-	6	-	pF
	Differential Gain	dg	at 3.58 MHz or 4.43 MHz	-	-	0.07	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	-	0.035	degrees
	All hostile crosstalk (see graph)	$X_{TALK\ (AH)}$	Sweep on 7 inputs 1V p-p 8th input has 37.5Ω resistor to gnd. f = 5 MHz	-	90	-	dB
	Chip disabled crosstalk (see graph)	$X_{TALK\ (CD)}$	Crosspoint on output to gnd. f = 10 MHz	110	-	-	dB

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

Monolithic 8x1 Video Crosspoint Switch with μP Interface

GX428 ADVANCE INFORMATION NOTE

VBD 10

FEATURES

* low differential phase and gain
* low crosstalk and high off-isolation
* I/O control of address and chip select
* 28 pin PLCC

CIRCUIT DESCRIPTION

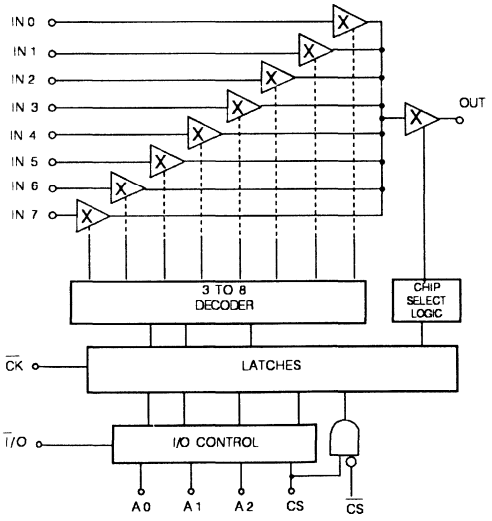
The GX428 is a bipolar high performance 8x1 multiplexer for use in video routing systems. It is characterized by being fully buffered, having make-before-break switching and low switching transients.

The device has on-chip I/O which allows the address and chip select to be read from the latches.

APPLICATIONS

* High quality Video Routing
* CCTV/CATV/monitor switching

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

I/O	A2	A1	A0	CS	CS	CLOCK	OUT
X	X	X	X	0	X	0	HI-Z
X	X	X	X	X	1	0	HI-Z
0	0	0	0	1	0	0	IN 0
0	0	0	1	1	0	0	IN 1
0	0	1	0	1	0	0	IN 2
0	0	1	1	1	0	0	IN 3
0	1	0	0	1	0	0	IN 4
0	1	0	1	1	0	0	IN 5
0	1	1	0	1	0	0	IN 6
0	1	1	1	1	0	0	IN 7
1	See note 1.					1	X
X	X	X	X	X	X	▲ 1	maintains previous state

NOTES: 1. When I/O is 1, the pins A0, A1, A2 and CS become outputs and reflect the contents of the latches.
2. When the clock is low, the latches are transparent.
3. X = don't care.

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Monolithic 16x1 Video Crosspoint Switch

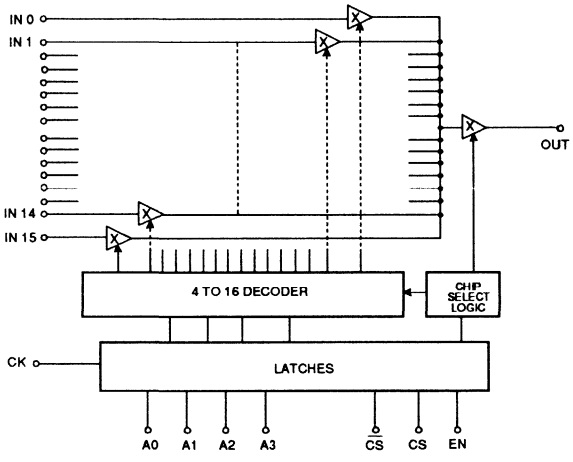
GX416 TENTATIVE DATA SHEET

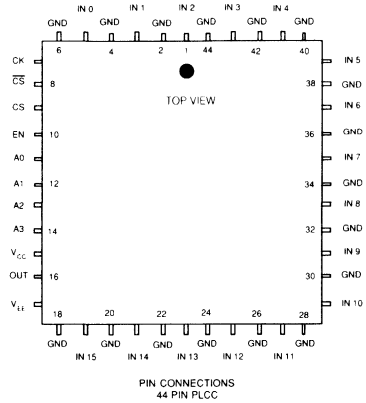
VBD 11

FEATURES

* low cost
* microprocessor compatible control logic
* differential phase at 3.58 MHz, 0.02° max. at ±12 V supply.
* differential gain at 3.58 MHz, 0.04% max. at ±12 V supply.
* off-isolation better than 120 dB at 10 MHz
* all hostile crosstalk 90 dB (typ.) at 5 MHz.
* gain spread at 8 MHz, ±0.05 dB max.
* insertion loss at 100 kHz, 0.05 dB (typ.)
* 44 pin quad, j-lead plastic package.
* low disabled power consumption, 7mW typ. at ±5V supply.

FUNCTIONAL BLOCK DIAGRAM





PIN CONNECTIONS
44 PIN PLCC

CIRCUIT DESCRIPTION

The GX416 is a microprocessor-compatible 16x1 video multiplexer featuring broadcast quality specifications, implemented in bipolar monolithic technology.

For use in dense NxM routing matrices, the GX416 features very high, nearly constant input impedance, coupled with very high output impedance in the disabled state. This allows multiple GX416 devices to be paralleled at the inputs and output without additional circuitry. The fully buffered unilateral signal path ensures negligible output-to-input feedback while delivering minimal output switching transients through make-before-break switching.

The logic inputs provide direct interfacing to microprocessor controllers, and are TTL and 5V CMOS compatible. True and inverse chip select inputs allow simple multiplexing of two or more GX416 devices.

The GX416 operates over a power supply range from ±4.5 to ±13.2 volts.

APPLICATIONS

* high density video routing switchers
* video production and master control switchers
* CCTV/CATV
* PCM/data routing matrices

TRUTH TABLE

EN	CS	CS	CK	A3	A2	A1	A0	OUT
1	1	0	1	0	0	0	1	IN 1
1	1	0	1	0	0	1	1	IN 3
1	1	0	1	0	1	0	1	IN 5
1	1	0	1	0	1	1	1	IN 7
1	1	0	1	1	0	0	1	IN 9
1	1	0	1	1	0	1	1	IN 11
1	1	0	1	1	1	0	1	IN 13
1	1	0	1	1	1	1	1	IN 15
X	0	X	1	X	X	X	X	HI Z
X	X	X	▼	X	X	X	X	multiplexer maintains previous condition

X = don't care.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5 V
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-65°C \le T_S \le 150°C$
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	$-4V \le V_{IN} \le 6V$ or $V_{CC}+0.3V$
Logic Input Voltage	$0V \le V_L \le 5.5V$

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, R_L = 10KΩ, C_L = 30pF)

PARAMETER	SYMBOL	VS = CONDITIONS	±5V MIN	±5V TYP	±5V MAX	±8V MIN	±8V TYP	±8V MAX	±12V MIN	±12V TYP	±12V MAX	UNITS
Supply Voltage	$\pm V_S$		4.5	-	-	-	-	-	-	-	13.2	V
Supply Current	I+	Chip selected ($\overline{CS}$=0)	-	12	-	-	12	-	-	12	-	mA
		Chip not selected ($\overline{CS}$=1)	-	1.2	-	-	1.7	-	-	2.4	-	mA
	I-	Chip selected (CS=0)	-	11	-	-	11	-	-	11	-	mA
		Chip not selected ($\overline{CS}$=1)	-	0.22	-	-	0.23	-	-	0.25	-	mA
Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs										V
Analog Input Bias Current —	I_{BIAS}		-	22	-	-	22	-	-	22	-	µA
Output Offset Voltage	V_{OS}	t_A = 25°C, 75Ω resistor on each input to gnd	-12	0	+12	-12	0	+12	-12	0	+12	mV
Output Offset Voltage Drift —	$\Delta V_{OS} / \Delta T$		-	-	200	-	-	200	-	-	200	µV/° C
Crosspoint Selection Turn-On Time	t_{ADR-ON}	Control input to appearance of signal at output	-	500	-	-	500	-	-	500	-	ns
Chip Selection Turn-On Time	t_{CS-ON}	Control input to appearance of signal at output	-	750	-	-	750	-	-	750	-	ns
Strobe Pulse Width	t_{PW}		200	-	-	200	-	-	200	-	-	ns
Logic Input Thresholds	V_{IH}	1	2.0	-	-	2.0	-	-	2.0	-	-	V
	V_{IL}	0	-	-	1.1	-	-	1.1	-	-	1.1	V
Logic Input Bias Current	I_{BIAS}	Chip selected A0, A1 = 1	-	40	100	-	-	100	-	-	100	µA

ELECTRICAL CHARACTERISTICS (continued) (V_{SS} = ±8V DC, 0°C < T_A < 70°C, R_L = 10kΩ, C_L = 30pF)

PARAMETER	SYMBOL	VS = CONDITIONS	±5V MIN	±5V TYP	±5V MAX	±8V MIN	±8V TYP	±8V MAX	±12V MIN	±12V TYP	±12V MAX	UNITS
DYNAMIC												
Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.04	0.06	0.1	0.04	0.055	0.09	0.035	0.05	0.08	dB
Bandwidth (-3dB)	B.W.		90	-	-	90	-	-	90	-	-	MHz
Gain Spread at 8MHz			-	-	±0.07	-	-	±0.06	-	-	±0.05	dB
Input to Output Signal Delay Matching (chip to chip)	Δt	T_A = 25°C, R_G = 75 Ω, f = 3.579545 MHz	-	-	±0.08	-	-	±0.07	-	-	±0.06	ns
		0°C < T_A 70°C, R_S as above, f as above	-	-	±1.2	-	-	±1.1	-	-	±1.0	ns
Input Resistance	R_{IN}	Chip selected (CS=0)	900	-	-	900	-	-	900	-	-	kΩ
Input Capacitance	C_{IN}	Chip selected (CS=0)	-	2.0	-	-	2.0	-	-	2.0	-	pF
Output Resistance	R_{OUT}	Chip selected (CS=0)	-	14	-	-	-	14	-	14	-	Ω
Output Capacitance	C_{OUT}	Chip not selected (CS=1)	-	6	-	-	6	-	-	6	-	pF
Differential Gain	dg	at 3.58 MHz	-	-	0.01	-	-	0.07	-	-	0.04	%
Differential Phase	dp	V_{IN} = 40 IRE	-	-	0.1	-	-	0.035	-	-	0.02	degrees
All Hostile Crosstalk	$X_{TALK-ALL}$	Sweep on 15 inputs 1V p-p 16th input has 10 Ω resistor to gnd. f = 5MHz	77	86	-	80	88	-	82	90	-	dB
Chip Disabled Crosstalk	$X_{TALK-CD}$	14 Ω on output to gnd f = 10MHz	100	-	-	110	-	-	120	-	-	dB
Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0pF)	77	110	-	88	125	-	97	140	-	V / µs
	-SR		63	90	-	72	100	-	80	115	-	

VBD 11

GENNUM CORPORATION

Monolithic Wideband 8x1 and 16x1 Video Crosspoint Switches

GX4108/GX4116 ADVANCE INFORMATION

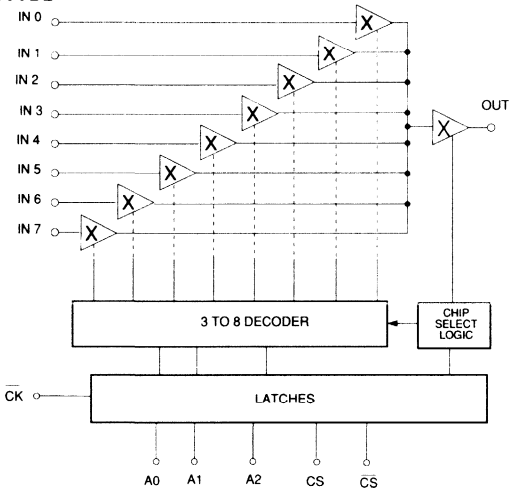
VBD 12

FEATURES

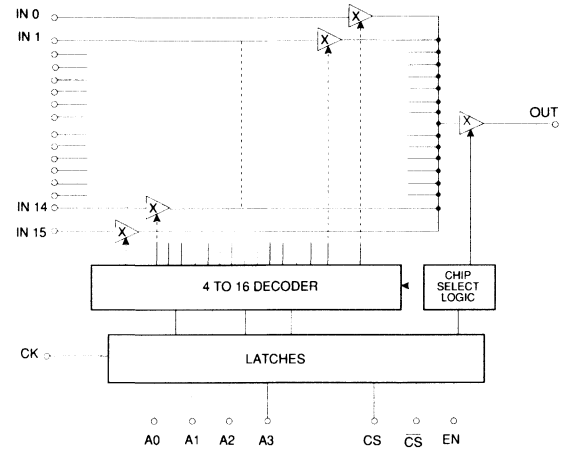
* low differential gain and phase
* wide bandwidth, -3dB at 300 MHz
* on-board decoding and latching logic

FUNCTIONAL BLOCK DIAGRAMS

GX4108



GX4116



CIRCUIT DESCRIPTION

The GX4108 and GX4116 are wideband video multiplexers implemented in bipolar monolithic technology. The GX4108 is an 8x1 while the GX4116 is a 16x1 multiplexer. These devices are characterized by excellent differential gain and phase in the enabled state, and a very high off-isolation in the disabled state. Fully buffered unilateral signal paths ensure negligible output to input feedback, while delivering minimal output switching transients through make-before-break switching.

For use in NxM routing matrices, these devices feature very high, nearly constant input impedance, coupled with very high output impedance in the disabled state. This allows multiple devices to be paralleled at the inputs and output without additional circuitry.

Both devices feature a microprocessor-compatible TTL and 5V CMOS control interface.

The GX4108 and GX4116 are members of the wideband video crosspoint family utilizing Gennum's proprietary LSI process.

APPLICATIONS

* very high quality video switching
* very high density video switching
* computer graphics
* high definition TV
* PCM/data routing matrices

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TRUTH TABLES

GX4108

A2	A1	A0	CS	$\overline{CS}$	$\overline{CK}$	OUT
X	X	X	0	X	0	HI-Z
X	X	X	X	1	0	HI-Z
0	0	0	1	0	0	IN 0
0	0	1	1	0	0	IN 1
0	1	0	1	0	0	IN 2
0	1	1	1	0	0	IN 3
1	0	0	1	0	0	IN 4
1	0	1	1	0	0	IN 5
1	1	0	1	0	0	IN 6
1	1	1	1	0	0	IN 7
X	X	X	X	X	↑	multiplexer maintains previous state
X	X	X	X	X	1	

X = don't care.

GX4116

EN	CS	$\overline{CS}$	CK	A3	A2	A1	A0	OUT
1	1	0	1	0	0	0	0	IN 0
1	1	0	1	0	0	0	1	IN 1
1	1	0	1	0	0	1	0	IN 2
1	1	0	1	0	0	1	1	IN 3
1	1	0	1	0	1	0	0	IN 4
1	1	0	1	0	1	0	1	IN 5
1	1	0	1	0	1	1	0	IN 6
1	1	0	1	0	1	1	1	IN 7
1	1	0	1	1	0	0	0	IN 8
1	1	0	1	1	0	0	1	IN 9
1	1	0	1	1	0	1	0	IN 10
1	1	0	1	1	0	1	1	IN 11
1	1	0	1	1	1	0	0	IN 12
1	1	0	1	1	1	0	1	IN 13
1	1	0	1	1	1	1	0	IN 14
1	1	0	1	1	1	1	1	IN 15
0	X	X	1	X	X	X	X	HI Z
X	0	X	1	X	X	X	X	HI Z
X	X	1	1	X	X	X	X	HI Z
X	X	X	↓	X	X	X	X	multiplexer maintains previous state
X	X	X	0	X	X	X	X	

X = don't care.

GENNUM CORPORATION

Fast Toggling Video Crosspoint Switch

GY4102 TENTATIVE DATA SHEET

VBD 13

FEATURES

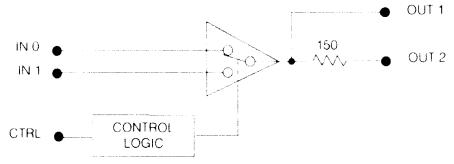
* 25 ns switching time (toggle)
* make-before-break switching
* 200 MHz at -3dB, bandwidth
* typically 0.025 dB insertion loss at 1 MHz
* less than 0.1 % differential gain at 3.58 MHz
* less than 0.1 degree differential phase at 3.58 MHz

CIRCUIT DESCRIPTION

The GY4102 is a bipolar, monolithic SPDT video switch incorporating fast control logic. The analog signal path is characterised by low differential gain, low differential phase and low insertion loss, coupled with a -3 dB bandwidth of typically 200 MHz into a 10 pF load.

Fast set-up times in the order of 20 nanoseconds allow toggling of video or data up to 20 MHz. The control input is TTL and 5 V CMOS compatible. The GY4102 is available in an 8 pin DIP.

FUNCTIONAL BLOCK DIAGRAM



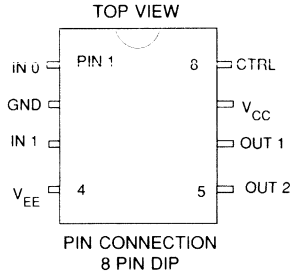
APPLICATIONS

* Sub-pixel video switching
* Fast data sampling
* Modulation
* Special Effects video switching

TRUTH TABLE

CTRL	OUTPUT*
0	IN 0
1	IN 1

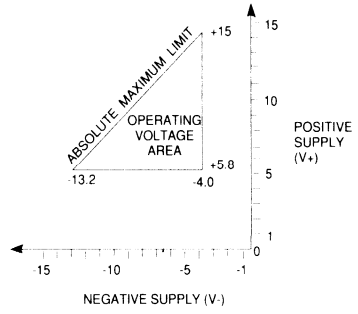
* 1 or 2



PIN CONNECTION
8 PIN DIP

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Positive Supply Voltage	+14.5 V
Negative Supply Voltage	-13.2 V
Maximum Supply Voltage Differential (V+ to V-)	19 V
Operating Temperature Range	0°C to 70° C
Storage Temperature Range	-65°C to 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage (IN 0, IN 1)	-2.5 V to +3.5 V
Control Input Voltage Range	$-4 < V_{CTRL} <$ $V_{CC}+0.3$ V or +7.0 V



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ELECTRICAL CHARACTERISTICS (V_{CC} = ±5V DC, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I+			-	10	-	mA
	I-			-	10	-	mA
Normal Supply Voltages	Vs	±5, +12 / -5, +5 / -12					V
Switch Turn-on/off Delay	$td_{ON/OFF}$			-	20	25	ns
Switching Transients		Duration is typically 10 ns unfiltered		-	-	80	mVpeak
Control Input Bias	I_{CTRL}	Control = 1		-	5	-	µA
Logic Level threshold	V_{LOGIC}		1	2	-	-	V
			0	-	-	1.1	V
Signal Input Bias	I_{SIG}			-	5	-	µA
Insertion Loss	I.L.	f = 1 MHz		-	0.02	-	dB
		f = 10 MHz		-	-	0.05	dB
Differential Gain	dg	f = colorburst	±5V	-	0.05	0.1	%
		3.58 or 4.43 MHz	±8V	-	0.025	0.05	
Differential Phase	dp	f = colorburst	±5V	-	0.05	0.1	degrees
		3.58 or 4.43 MHz	±8V	-	0.01	0.025	
Crosstalk	XTALK	f = 3.58 MHz		-	80	-	dB
Bandwidth	f_{3dB}	C_L = 10 pF		100	-	-	MHz
Output Voltage Swing	V_O			-2	-	+3	V

AVAILABLE PACKAGING

8 pin DIP

CAUTION

ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE DEVICES EXCEPT AT A STATIC-FREE WORKSTATION

Frequency Peaking Compensation of the GX414 and GX424

by J. Ian Ridpath, Senior Applications Engineer, Video/Broadcast Products

APPLICATION NOTE

VBA 1

INTRODUCTION

In video switching applications, the crosspoint switch must meet several critical specifications which include differential phase, differential gain and frequency response flatness. The GX4 family of crosspoint switches exceed broadcast requirements for the above specifications. For wide bandwidth and high bit rate data applications, the frequency/flatness performance of these devices can be easily extended using information in this application note. Information presented gives the system designer two methods of frequency compensating a system using the GX414 and GX424 Video Crosspoint Switches.

The first method uses a small value series resistor placed in the output of each device. The second method utilises the frequency roll-off characteristics of the external video buffer amplifier.

CHARACTERISTICS OF THE GX414 AND GX424

The GX414 and GX424 are bipolar video crosspoint switches configured as shown in Figure 1. Each analog switch has an emitter follower input, some level shifting and clamping circuits and an emitter follower output. The four switch outputs are tied together and brought out to one common pin. At frequencies above 1 MHz, the emitter follower switches naturally exhibit frequency response peaking.

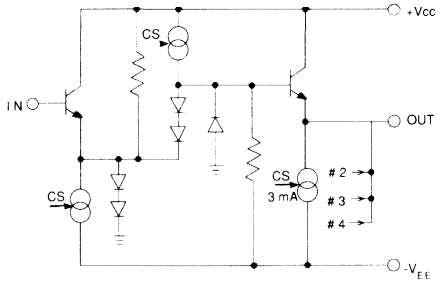

Fig.1 Enabled Crosspoint Equivalent Circuit

The output impedance is roughly modelled as shown in Fig. 2.

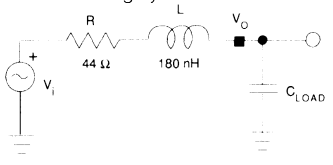

Fig.2 Output Impedance Model

The transfer function of this network is:

$$T_S = \frac{V_O}{V_I} = \frac{\frac{1}{LC}}{s^2 + s\left(\frac{R}{L}\right) + \frac{1}{LC}} \quad \ldots\ldots 1$$

This transfer function has a pair of complex conjugate poles with

$$f_O = \frac{1}{2\pi\sqrt{LC}} \quad \ldots\ldots 2$$

and

$$Q = \left(\frac{1}{R}\right)\left(\sqrt{\frac{L}{C}}\right) \quad \ldots\ldots 3$$

The frequency response peaks when $Q > 1/\sqrt{2}$ at a frequency equal to f_O, but it is maximally flat when $Q = 1/\sqrt{2}$.

In the above equations, the capacitance C, represents the load capacitor external to the device. With any value of C, a value of R can be found which will make $Q = 1/\sqrt{2}$, thus flattening the response. Practically, this can be accomplished by placing an external resistor in series with the output of the device.

In video routing or matrix switching applications, the load capacitance on the output bus is determined by how many devices are connected to the bus. A typical example as shown in Figure 3, uses five GX414s or five GX424s wired as a 20 x 1 matrix.

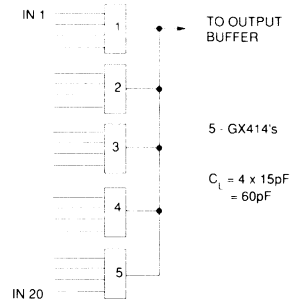

Fig.3 20 x 1 Matrix

For any single selected crosspoint, four of the devices will be disabled and one will be enabled (selected). The output capacitance of a disabled device is approximately 15 pF resulting in the total load capacitance seen by the selected device as approximately 60 pF. Assuming stray capacitance adds a further 5 pF to the system output, the total external capacitance will be approximately 65 pF.

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Method 1. Adding Series Resistance to the Output

Using equation 3), the value of R which will cause Q to equal $1/\sqrt{2}$ will be;

$$R = (\sqrt{2}) \cdot \frac{\sqrt{180\ nH}}{\sqrt{65pF}} \text{ ohms}$$

which yields; R = 74.4 ohms

Since the equivalent series output resistance of the device is 44 Ω (as shown in Figure 2), an additional 30.4 Ω must be added in series with the output in order to make the total resistance equal to 74.4 Ω. Figure 4 shows the frequency response of the above set-up along with the uncompensated response. For this graph, a 33 Ω resistor was used and a 60 pF load capacitor simulated the additional disabled devices.

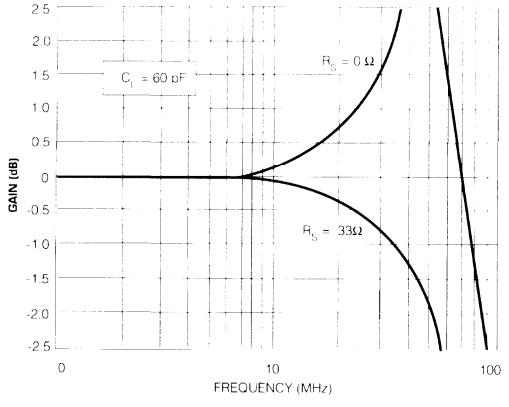


Fig. 4 Frequency and Uncompensated Responses

With the same 33 Ω resistor in the circuit, the load capacitors were changed to 47 pF and 27 pF in order to see their effects on the frequency response. The 47pF capacitor closely simulates a 16 x 1 crosspoint circuit while the 27 pF approximates a 10 x 1 situation. Figure 5 shows the results of these changes.

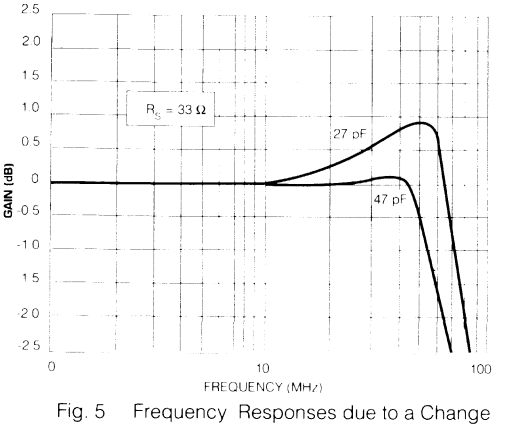


Fig. 5 Frequency Responses due to a Change of Capacitor Values

Precise modelling has been done yielding far more accurate results. The effect on the frequency response of any series compensating resistor can be computer simulated using these models. Figure 6 is an engineer-generated model of the GX414 or GX424 device. This model has been simulated using 'PSpice' (software by MicroSim Corporation) and compared to measured results. A PSpice NETLIST is available on floppy disk from Gennum for assisting the systems engineer and designer. The input and output impedance parameters are specified for frequencies up to 70 or 80 MHz and will produce accurate frequency response results for load capacitances between 10 pF and 100 pF.

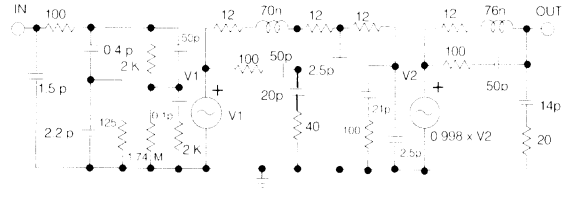


Fig. 6 Engineer-generated Model of GX414 or GX424

Figure 7 is an approximate model of a disabled crosspoint switch showing some of the circuit potentials and more importantly, the various capacitances associated with a disabled switch.

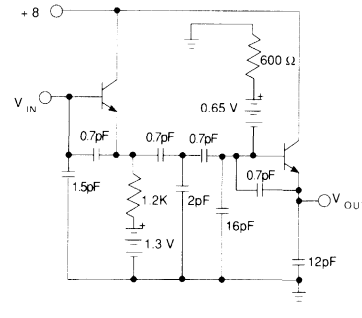


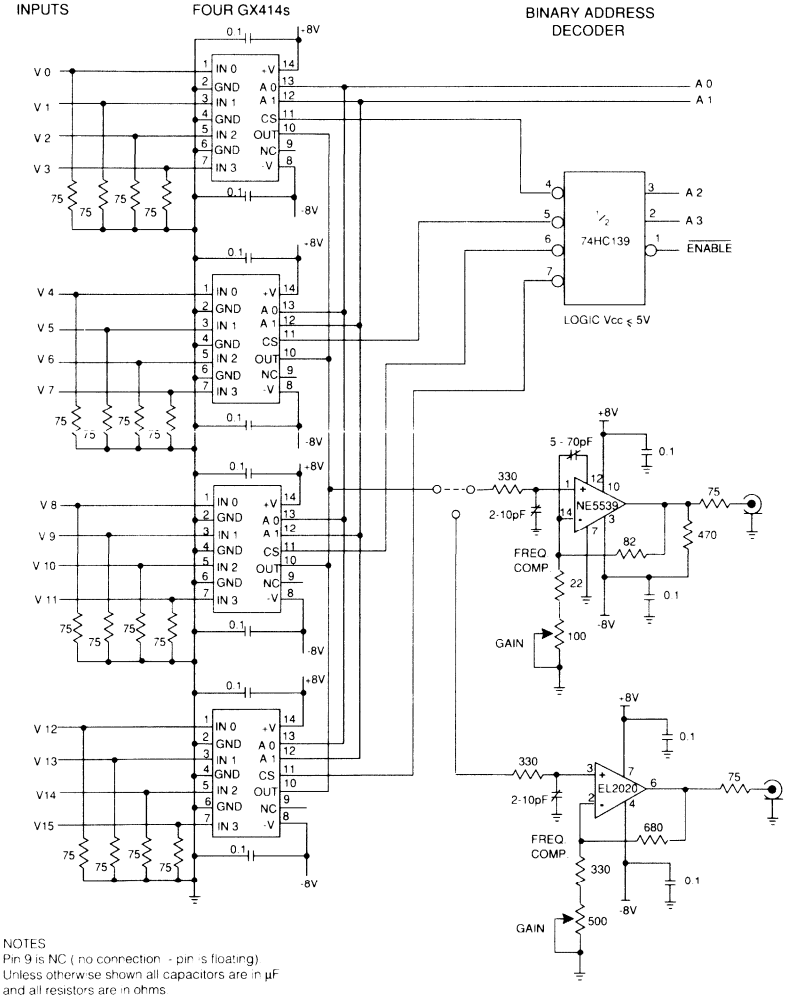
Fig. 7 Disabled Crosspoint Equivalent Circuit

The input capacitance of a disabled switch varies with the DC bias voltage from 2.1 pF at -1 volt to 2.5 pF at +1.5 volts. Futhermore, there is a slight change in C_{IN} between the disabled state (2.2 pF at 0 volts bias) and enabled state (2.0 pF at 0 volts bias). The slight variations would only be significant if the input driver source impedance is high. The output capacitance of the disabled chip is made up of four times 0.7 pF, for the four output transistors, plus 12 pF which is common to all outputs, giving a total of approximately 15 pF.

Method 2. Frequency Compensation by the Output Buffer Stage.

The only drawback of using a series resistor to compensate for the peaking response of the GX414 and GX424 is the slight degredation of differential phase through the switch and resistor. Since the outputs are eventually buffered at the bus by an operational amplifier or a specifically designed video buffer, it seems reasonable to compensate at this point in the system.

Figure 8 shows a 16 x 1 system that is set up using four GX414's and two popular buffer amplifiers. The first is an Élantec EL-2020 and the second is a Signetics NE-5539. The EL-2020 is a 50 MHz current feedback amplifier specifically designed for use in video applications. The NE-5539 is an ultra-wideband operational amplifier having an external frequency compensation pin.



NOTES
Pin 9 is NC (no connection - pin is floating)
Unless otherwise shown all capacitors are in µF
and all resistors are in ohms.

Fig. 8 16 x 1 Video Crosspoint Circuit

Several combinations of resistor values were used in order to set the gain of each amplifier to 6 dB and yet maintain stability. A small trimmer capacitor in conjunction with a series resistor was used as a lag-circuit at the amplifier input. Along with this circuit, in the case of the NE-5539, a compensating trimmer capacitor was connected to the compensation pin.

Each buffer amplifier was then independently connected to the 16 x 1 crosspoint circuit and the variable circuit elements were adjusted to flatten the frequency response. The frequency response was observed and measured using the test set-up as shown in Figure 9.

Initially, the buffer amplifiers were set up having as wide a bandwidth as possible. Results approaching those shown in the manufacturer's data book were achieved. The crosspoint switches were then placed in the circuit and obvious amounts of frequency peaking were noticed.

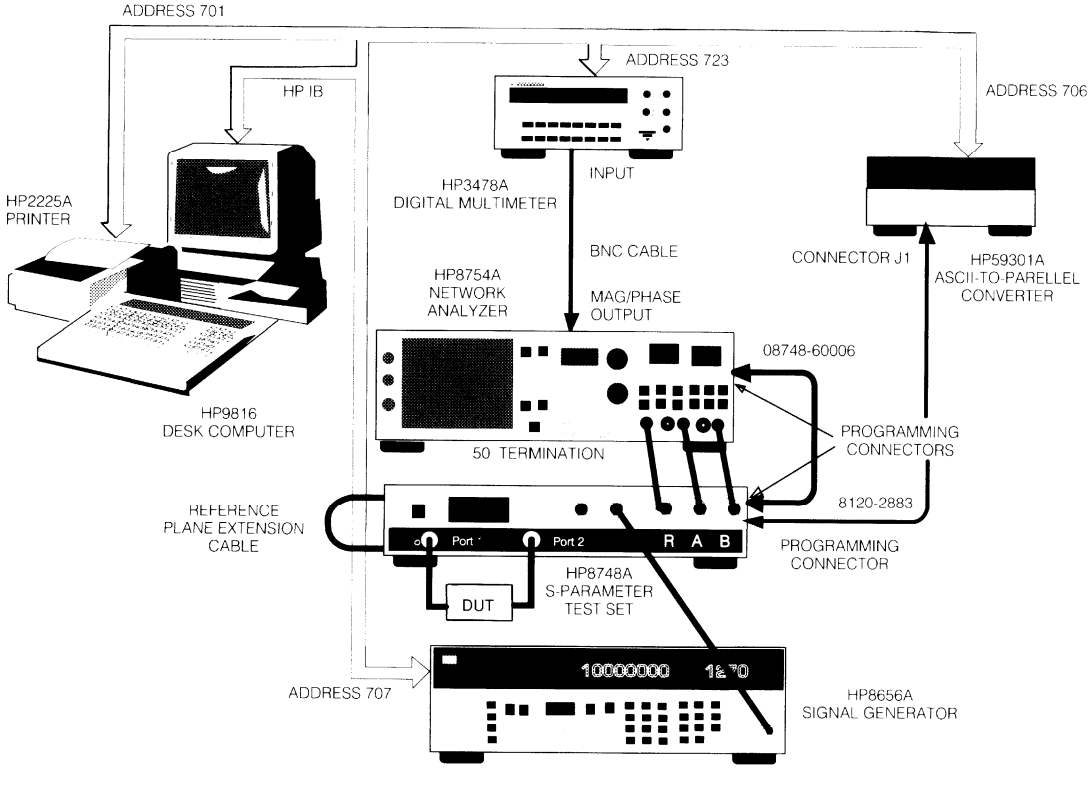


Fig. 9 Test Set-up

The lag-circuit trimmer, the compensating trimmer and gain potentiometers were adjusted until a flat response was achieved. Figures 10, 11 and 12 show the various frequency response results.

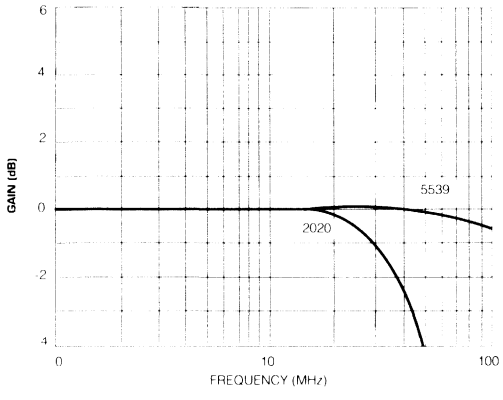


Fig. 10 Amplifier Response

The wide bandwidth of the NE5539 is obvious with a -3dB frequency of well over 200 MHz, while the -3dB point of the EL-2020 is about 45 MHz.

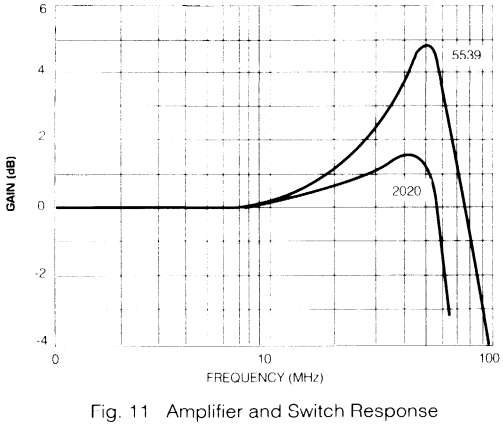


Fig. 11 Amplifier and Switch Response

Predictable peaking occurs in both systems between 40 and 50 MHz.

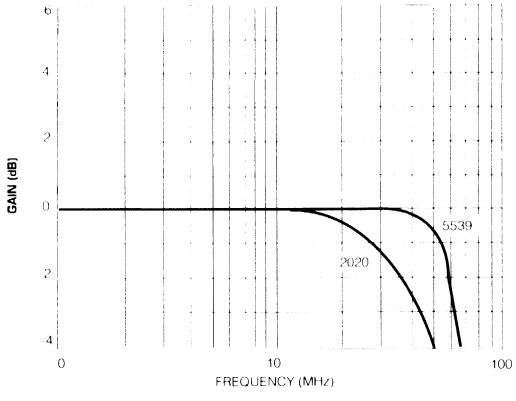


Fig. 12 Resultant Flat Response

Virtually all peaking has been removed, resulting in a flat response to at least 35 MHz for the NE5539 and at least 15 MHz for the EL-2020.

CONCLUSION

This brief application note has dealt with the compensation for flatness that is necessary when using the GX414 and GX424 video crosspoint switches. The video system designer is concerned with flatness and insertion loss of any crosspoint switch in his system at the colour burst frequencies of either 3.58 MHz or 4.43 MHz.

The insertion loss of the GX4 family of devices at these frequencies in less than 0.05 dB. However, for wideband and high bit rate data, it is important to have a flat response, out to at least 30 to 50 MHz. Using the techniques described in this application note in conjunction with the buffer stages specified, the GX414 and GX424 switches can be made to have a flat response up to the frequencies mentioned above.

Indeed, the peaking response of the GX414 and GX424 can be used to advantage with a falling response found in most operational amplifier circuits in order to flatten the overall frequency response.

Application engineers at Gennum are more than happy to work along with system designers and will try to answer any customer questions regarding the GX414 and GX424, high performance Video Crosspoint Switches.

GENNUM CORPORATION

Comparison of 4x1 Video Crosspoint Switches

by Ian Ridpath, Senior Applications Engineer, Video/Broadcast Products

INFORMATION NOTE

A Look at Parameter and Operating Differences Between the GX414, GX414A, GX424 and GX434 Monolithic, Bipolar, 4x1 Video Crosspoint Switches

VBA 2

INTRODUCTION

It is perhaps worthwhile, before looking into the differences, to view the similarities between members of this family of high performance video crosspoint switches. Functionally, all the devices represent a 4x1 crosspoint configuration as shown in Figure 1.

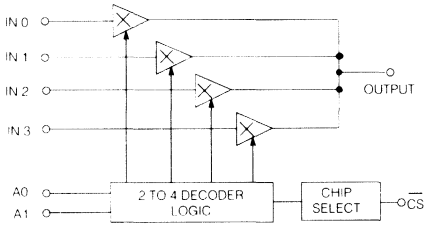


Fig. 1 Functional Diagram

They are all pin-for-pin compatible with the exception of the GX434 which uses the normally unused pin 9 as a connection point for an external 1% resistor. They are all available in standard 14 pin DIP and 16 pin SOIC packages.

The data sheets provide detailed electrical parameter specifications and performance graphs for each device. This information note looks specifically at the differences in some of the parameters, how they are achieved, and their effect on the selection of a member of this family group for a particular application.

DEVICE COMPARISONS

COMPARISON 1: GX424 vs GX414

The GX424 is identical in all operating respects to the GX414; only the *'test program'* varies for each device, in order to allow the GX424 to pass with wider parameter spreads and reduced specifications. These wider spreads and reduced specifications are compared in Table 1.

PARAMETER	UNITS	GX424	GX414
Maximum supply current	(mA)	18	14
Output offset voltage range	(mV)	-20 to +30	-2 to +12
Maximum offset drift	µV/°C	+300	+200
Input to output delay spread at 25°C (chip-to-chip)	(deg)	±0.80	±0.35
Address logic (turn-on time)	(ns)	100 to 350	130 to 270
Chip selection (turn-on time)	(ns)	150 to 450	200 to 400
Maximum differential gain	(%)	0.1	0.05
Maximum differential phase	(deg)	0.05	0.025
Max. insertion loss at 10 kHz	(dB)	0.06	0.05
Minimum 3 dB bandwidth (C_L = 30 pF)	(MHz)	80	90
Gain spread at 8 MHz (C_L = 30 pF)	(dB)	+0.46 -0.12	±0.1
Min. OFF isolation at 10 MHz	(dB)	90	100
Min. all hostile crosstalk at 5 MHz	(dB)	92	94
Minimum slew rate (C_L = 0 pF)	(V/µs)	+60 -50	+84 -70
Relative cost		lower	

Table 1

The video system designer has the choice of using either the GX414 or GX424 depending whether or not, for the sake of cost-effectiveness, a sacrifice in performance is warranted.

COMPARISON 2: GX414A vs GX414

Nearly all parameters are the same for the two devices. The exceptions are shown in Table 2. (see over)

An additional processing stage (on-chip capacitance) compensates for frequency peaking but reduces the slew rate.

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PARAMETER	UNITS	GX414A	GX414
Input to output signal delay matching (chip-to-chip)	(deg)	±0.6	±0.35
Gain spread at 8 MHz	(dB)	±0.25	±0.1
Typical slew rate (C_L = 0 pF)	(V/µs)	±40	+120 -100
Relative cost		higher	

Table 2

COMPARISON 3: GX434 vs GX414

The parameters and operating characteristics of the GX434 most closely resemble the GX414. The normally unused pin 9 is now employed for connecting an external precision resistor. The parameter differences between the two devices are tabulated in Table 3.

PARAMETER	UNITS	GX434	GX414
Input to output signal delay matching chip-to-chip			
at T_A = 25°C	(deg)	±0.15	±0.35
at Full temp.range	(deg)	±0.3	±0.7
Max. supply current	(mA)	11.5	14
Min. 3 dB bandwidth (C_L = 30 pF)	(MHz)	100	90
Gain spread at 8 MHz	(dB)	+0.06 - 0.04	±0.1
Typical slew rate (C_L = 0 pF)	(V/µs)	+450 -200	+120 -100

Table 3

This higher degree of delay matching and gain spread is achieved by using an external 33.2 kΩ, 1% resistor connected to pin 9. All the other 4x1 devices compared in this note use an onboard resistor which has a tolerance of between 20 and 25 percent. These resistors effectively control currents within the chip that determine the input-to-output signal delay. The tighter the control of the resistor tolerance, the less is the chip-to-chip delay spread.

The difference in the frequency response values and slew rate are due to a modification to the on-chip frequency peaking compensation network.

CONCLUSIONS

Even though this particular group of devices is similar in so many respects, the differences described are significant to the video systems designer. This is especially true if a cost-effective yet performance enhanced system is required.

The design and application engineers at Gennum are always happy to discuss system requirements for any of the video crosspoint switch ICs.

16x1 VIDEO CROSSPOINT EVALUATION BOARD

by Ian Ridpath, Senior Application Engineer, Video and Broadcast Products Group

APPLICATION NOTE

INTRODUCTION

This application note describes the construction and use of the GENNUM 16x1 Video Crosspoint Evaluation Board. This board is intended to demonstrate the straight forward application of the GX414, GX414A, GX424 and GX434 video crosspoint switches in a 16x1 multiplexer configuration.

DESIGN FEATURES

In addition to the crosspoint switches, this board incorporates address decoding and disable logic and an output buffer amplifier. With a total parts count of only 28 (excluding optional DIP sockets and I/O connectors), the Gennum 16 x 1 circuit represents the simplest, most cost effective and lowest power consumption 16 x 1 video crosspoint module available.
(See note 1, page 5)
Other features are highlighted below.

* Extremely low differential gain and phase (final result depends on buffer amplifier used).

* Extremely high OFF isolation and low crosstalk.

* Virtually no switching *glitches*.

* No external buffer transistors are needed in order to keep the ON to OFF input impedance constant.

* Less than 30 mW disabled power consumption

The on board video buffer allows the multiplexed video signal to directly feed a 75Ω load. An additional unbuffered video output allows the user to parallel up several boards and connect an external buffer.

THEORY OF OPERATION (refer to Figure 1)

Each crosspoint IC has a $\overline{\text{Chip Select}}$ and two Address inputs which operate according to the following truth table.

TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE

If more than one device is used, the ADDRESS inputs for each device are simply connected in parallel. The address selection bits are A0 and A1 and determine which of the four crosspoints per device are activated. However, until the chip has been selected (chip select = 0), no signal path exists.

The four $\overline{\text{Chip Select}}$ inputs must be decoded from the two most significant address bits, A2 and A3. Furthermore, all the devices must be turned off if none of the 16 video inputs (IN1 to IN16) are required (circuit disabled). This decoding and disabling is accomplished by one half of an MM74HC139N dual 2 to 4 decoder.

The two most significant address bits are applied to pins 2 and 3 of this device. When the device is enabled (low on pin 1), a unique low state output is generated at the output (pins 4, 5, 6 or 7). When the 74HC139 IC is disabled, (Disable = 1), all the outputs go high and turn off all four GX4 devices. In this manner any one of sixteen video paths can be selected or all can be turned off by using five bits of data (A0,A1,A2,A3 and Disable.)

The video input signals are directly connected to the video switches. If these signals are fed from a 75 Ω cable, a 75 Ω resistor should be installed from the input to ground. In multi-input applications where the input is driven from a low impedance buffer amplifier, these 75Ω resistors are not needed. All unused inputs should either be tied directly to ground or tied down with 75 Ω resistors.

Assuming that a video signal on input 1 (IN 1) is required to be switched to the output, the data bits should be as follows;

A0 = 0,
A1 = 0,
A2 = 0,
A3 = 0,
DISABLE = 0 (enabled).

In this case, the first of the four crosspoint switches in IC1 is selected by address bits A0 and A1. Pin 4 of IC5 goes low because address bits A2 and A3 are low and because pin 1 of the device is low (low = enable).

The low logic level coming from pin 4 of IC5, creates a chip selection for IC1, enabling the crosspoint and allowing the video signal on IN-1 to be routed to pin 10. From here it goes to the buffer amplifier, IC6 via the 22 Ω series resistor, R1 and a lag circuit made up of R5 and C12.

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The series resistors R1-R4 dampen the Q of the frequency peaking response of the crosspoint switches and the lag circuit further tailors the frequency response in order to produce a flat response (see note 2, page 5). The gain of the buffer is nominally set for 2 (+6 dB) by the trimpot, R9, in order to compensate for the loss through the 75 Ω back matching resistor, R8. Similarly, if the video signal on IN16 was selected, the data bits would have to have the following logic levels:

A0 = 1, A1 = 1, A2 = 1, A3 = 1, DISABLE = 0.

In this case, the fourth switch in IC4 would be activated and that chip would be selected by the low output on pin 7 of IC5.

Unbuffered video can be observed at the Unbuffered Video Output. When this output is used, a load resistance of 10 kΩ or greater should be used. The frequency response will be relatively flat up to 40 MHz or 50 MHz and is not dependent upon the response of the on board buffer.

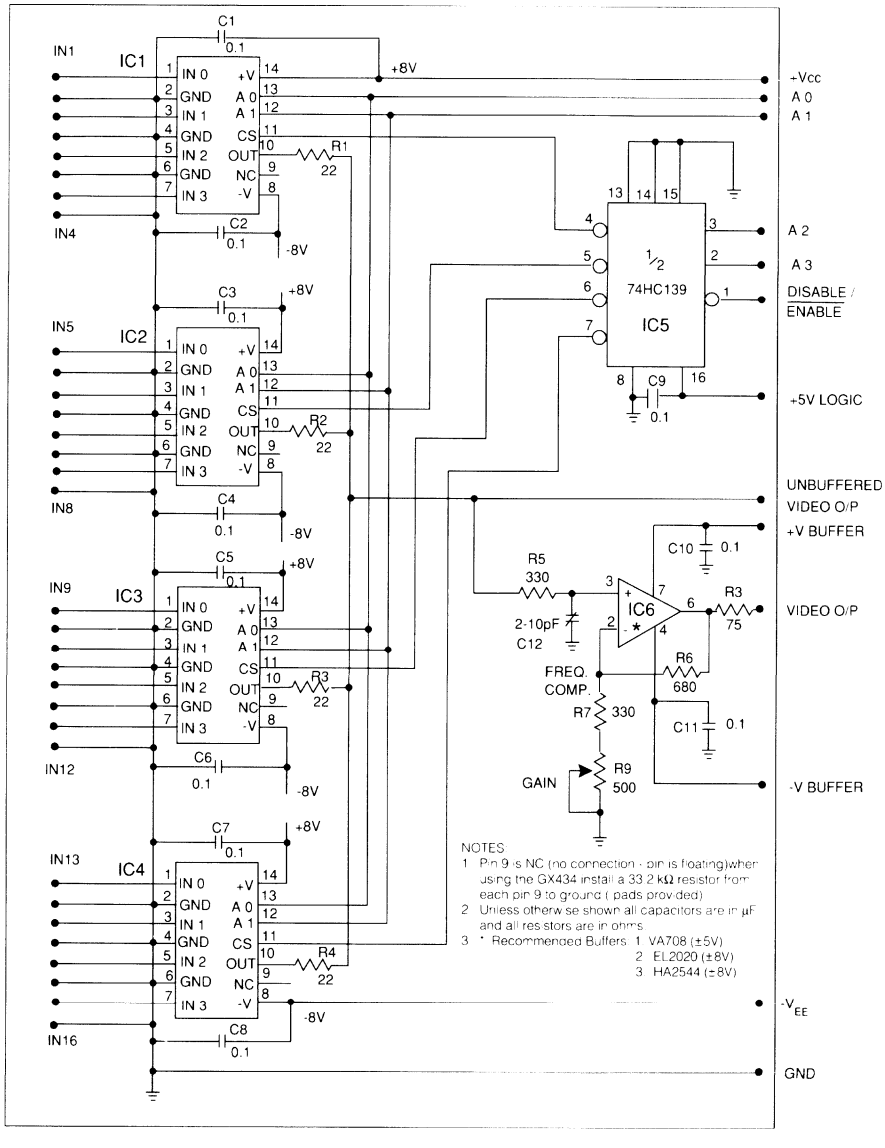


Figure 1 Circuit Diagram of the 16 x 1 Video Multiplexer Board

The power supply connections for the video buffer amplifier are independent of the rest of the circuit. The board is laid out to accept any of several video buffer amplifiers having the standard opamp pin-outs as shown. Many of these can operate from the same V_{CC} and V_{EE} as does the rest of the board. One amplifier recommended however, is the VA708 video buffer from VTC which has a maximum supply voltage rating of only 6 volts.

The power supply voltage for the logic must not exceed 5.25 volts. This allows the use of either LS-TTL or 5 volt HCMOS. There is however, an increase of 35 mW power consumption when LS-TTL is used.

CONSTRUCTION AND SET-UP

Artwork for the PCB is included in this application note along with a parts list and typical performance results. Construction is straight forward and should present no real problems. An etched and drilled PCB is available from Gennum Corporation at a nominal price. Those interested in obtaining a board should contact the Video/Broadcast Products Group at Gennum.

Two possible test set-ups are described in this application note. They are shown in Figures 2 and 3. One uses the on-board buffer amplifier and the other is for use with an external buffer. In either case, the address and enable logic levels can be generated by DIP switches or the outputs of shift registers and/or latches. If DIP switches are used, pull-up resistors must be included.

Also, if the buffer amplifier is capable of operating at the same supply voltages as the crosspoints, the appropriate supply pins can be wired together. This would leave only the logic portion of the board requiring a separate supply.

Figure 4 shows the placement of the components on the PCB

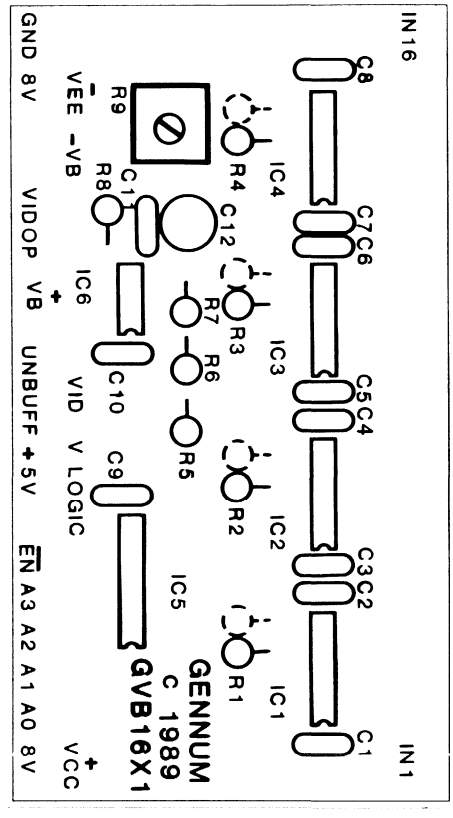


Fig. 4 Component Layout

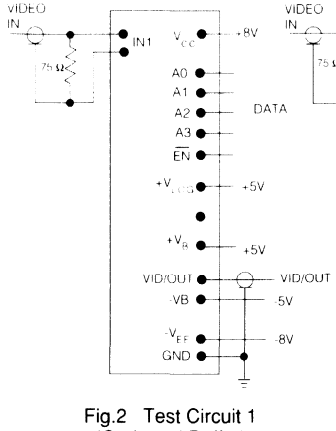


Fig.2 Test Circuit 1
(On-board Buffer)

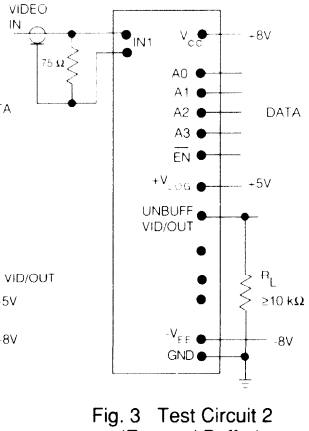


Fig. 3 Test Circuit 2
(External Buffer)

NOTE: -VB may be connected to $-V_{EE}$
+VB may be connected to $+V_{CC}$

Parts List

Qty	Description	Designation
1	Printed Circuit Board Gennum Corp.(GVB16X1)	
4	GX414CD IC Gennum Corp.	C1 to IC4
1	MM74HC139N IC National	I C5
1	VA708 or EL2020 or HA2544 video buffer IC	I C6
11	0.1 µF,100 V block capacitor	C1 to C11
1	2 to 10 pF trimmer capacitor	C12
4	22Ω, 1/4W, 1% resistors	R1 to R4
2	330Ω, 1/4W, 1% resistors	R5, R7
1	680Ω, 1/4 W, 1% resistor	R6
1	75Ω, 1/4W, 1% resistor	R8
1	500ΩPCB mount trimpot	R9
4	14 pin DIP sockets (optional)	
1	16 pin DIP socket (optional)	
1	8 pin DIP socket (optional)	
4	8 way strip connectors (0.1 in.) (optional)	
13	PCB connector terminals (optional)	

Test Results

Using test circuit 1 with a VA708 buffer amplifier, the following quantities were measured and calculated:

Crosspoint supply voltage	=	± 8 V
Buffer amplifier supply voltage	=	±5 V
Logic supply voltage	=	+5 V
1. Positive crosspoint supply current (disabled)	=	1.65 mA
2. Negative crosspoint supply current (disabled)	=	1.00 mA
3. Positive crosspoint supply current (enabled)	=	11.42 mA
4. Negative crosspoint supply current (enabled)	=	10.74 mA
5. Logic supply current (74LS139)	=	7.00 mA
6. Logic supply current (MM74HC139)	=	0.10 mA
7. Buffer Amplifier positive supply curent	=	8.40 mA
8. Buffer amplifier negative supply current	=	8.40 mA
9. Total DISABLE power consumption (74LS139)	=	140 mW
10. Total ENABLED power consumption(75LS139)	=	296 mW
11. Total DISABLED power consumption (74HC139)	=	105 mW
12. Total ENABLED power consumption (74HC139)	=	262 mW
13. Frequency response - 0.1 dB	=	20 MHz
- 1.0 dB	=	32 MHz
- 3.0 dB	=	42 MHz

Using test circuit 2 with no on board buffer amplifier, the following quantities were measured and calculated.

Crosspoint supply voltage	=	± 8 V
Logic supply voltage	=	+ 5 V
1. Positive crosspoint supply current (disabled)	=	1.65 mA
2. Negative crosspoint supply current (disabled)	=	1.00 mA
3. Positive crosspoint supply current (enabled)	=	11.42 mA
4. Negative crosspoint supply current (enabled)	=	10.74 mA
5. Logic supply current (74LS139)	=	7.00 mA
6. Logic supply current (74HC139)	=	0.10 mA
7. Total DISABLED power consumption (74LS139)	=	56.2 mW
8. Total ENABLED power consumption (74LS139)	=	212 mW
9. Total DISABLED power consumption (74HC139)	=	21.25 mW
10. Total ENABLED power consumption (74HC139)	=	178 mW
11. Frequency response (crosspoints alone)		
IN 16 +2.0 dB	=	42 MHz
-1.0 dB	=	65 MHz
-3.0 dB	=	80 MHz

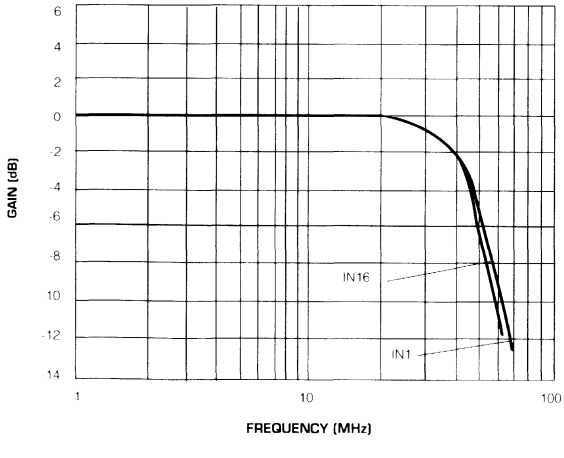


Fig.5 Frequency Response of Test Set-up 1

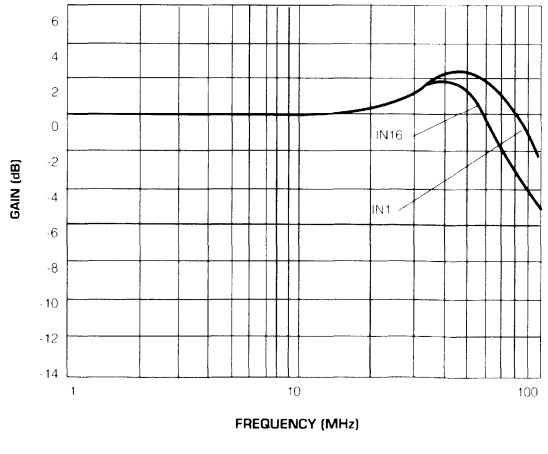
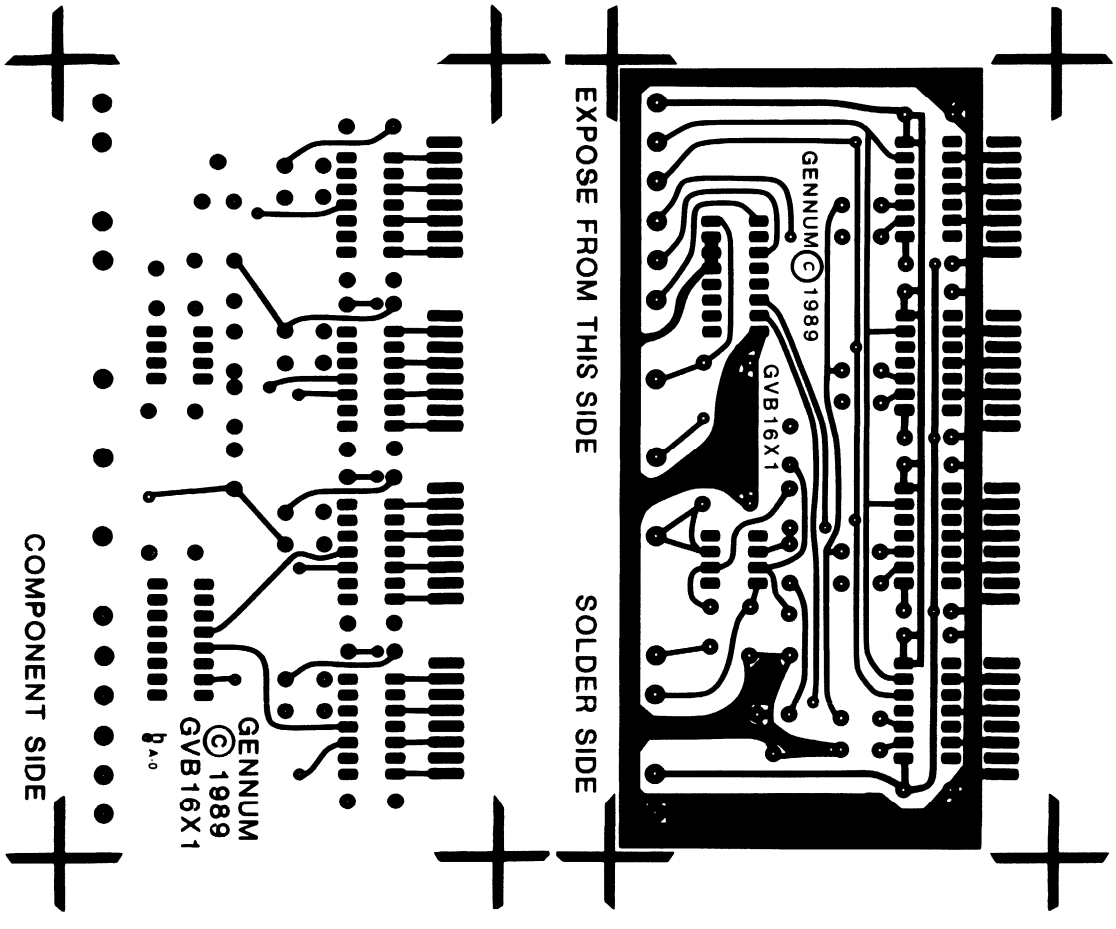


Fig.6 Frequency Response of Set-up 2

Printed Circuit Board Artwork



The artwork is a photographic copy at 82% of full size and may be reproduced and enlarged (122%). If plated through-hole facilities are not available, the pad-vias may be made by using tinned copper wire.

NOTES

1. Document 510-50 *A Comparison of Various 16 x 1 Video Switching Matricies.*
2. Document 510-39 Application Note *Frequency Peaking Compensation of the GX414 and GX424* (available from Gennum Corporation).

GENNUM CORPORATION

Comparison of 16x1 Video Multiplexer

by J. Ian Ridpath, Senior Applications Engineer, Video & Broadcast Products

INFORMATION NOTE

VBA 4

INTRODUCTION

This document presents comparative technical information between the Gennum GX414 video crosspoint switches and the various DCMOS products offered by Siliconix Inc. as used in 16x1 video multiplexer. The 16x1 configuration was chosen because it is quite often a basic building block found in many production switchers and routing systems.

No direct cost comparison has been made since the final assembled cost of a PCB varies, depending on whether standard or surface mounting techniques are used. However, a parts list is included for each circuit in order to allow the design engineer to cost each system on its own. The only assumption that has been made is that the best cost-effective solution (with highest performance specifications) is desired by the video design engineer.

The four circuits presented, compare the Gennum GX414 internally buffered bipolar 4x1 crosspoint to the Siliconix 16x1, 8x1 and 4x1 circuits represented by their DG536, DG538 and DG540 DCMOS integrated circuits.

THE GENNUM GX414 SOLUTION

The desired 16x1 configuration is simply implemented using four GX414 video crosspoint integrated circuits along with some address decoding and latching. No input buffer stages are needed with this circuit. The features of the Gennum solution are;

- extremely low differential phase and gain*
- extremely high isolation *
- no external transistors or resistors required
- minimal PCB board space (approximately 2" x 5")
- virtually no switching *glitches*
- virtually constant input capacitance (2.0 pF to 2.4 pF maximum variation).

Parts List

4	- GX414 IC (switches)
10	- Supply rail bypass capacitors
1	- 74HC139 IC (chip select decoder)
1	- MC14042 IC (quad latch)
2	- 16 way connectors (video inputs and grounds)
1	- 10 way connector (address/ enable/ strobe/ power and video out)
1	- PCB approx. 2" x 5"

Total parts count = 20

* See Gennum Data Sheet 510-38

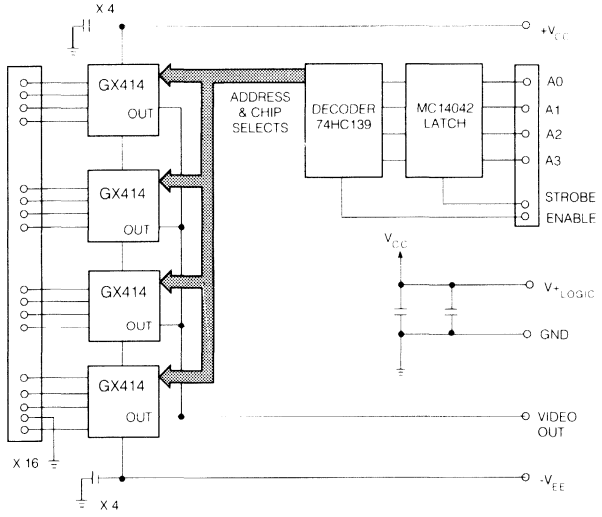


Fig. 1 Circuit Diagram of the 16x1 Multiplexer Using Four GX414 Devices

Document No. 510 - 51 - 2

THE SILICONIX DG-536 SOLUTION

This device has onboard address decoding and latching for all 16 switches. The logic inputs include Chip Select, Enable and Strobe, requiring virtually no external logic circuitry. When using split power supplies however, (for best differential phase and gain), the logic inputs must be level shifted.

The MOS bilateral channels require buffering at their inputs in order to prevent the flow of signal and switching transients from output to input. The buffers are also necessary in order to reduce the large capacitance change at the input of each switch from the ON to OFF condition of the channel.

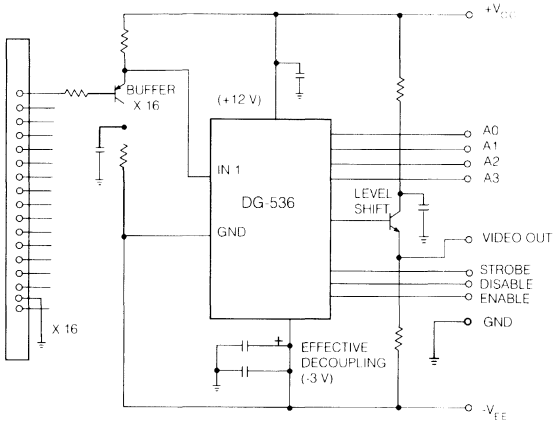


Fig. 2 Circuit Diagram of the DG-536 16x1 Multiplexer

A level shifting NPN transistor is also required at the output in order to restore the correct DC reference. It is usually necessary to clamp the output during switching. These transistors with their associated bias components and bypass capacitors take up more room than the integrated circuit itself resulting in a PCB of about 5 inches by 4 inches. The associated component cost, PCB area and manufacturing complexity does not make this arrangement as cost effective as the Gennum solution.

Parts List

1 - DG-536 IC (16 switches, decoder/latches etc.)
16 - PNP bipolar transistors (buffers)
1 - NPN bipolar transistor (output level shifter)
50 - Resistors for above transistors
20 - Supply bypass capacitors
2 - 16 way connectors (video inputs)
1 - 4 way connector (address)
1 - 6 way connector (power, video out, control)
1 - PCB - (5" by 4").

Total parts count = 93

THE SILICONIX DG-538 SOLUTION

This device is configured as an 8x1 analog switch having improved specifications over the DG-536. As with the DG-536, external input transistor buffers are required. Also, in order to make a 16x1 matrix, two DG-538 integrated circuits are necessary. A small amount of external logic is required in order to select each device. This circuit uses address bit A3 as the controlling signal along with an ENABLE signal that disables the entire 16x1 multiplexer.

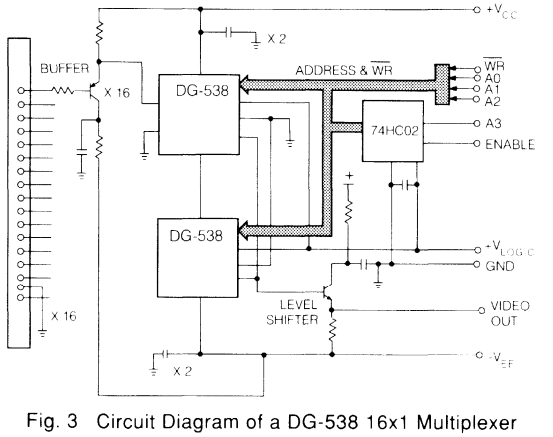


Fig. 3 Circuit Diagram of a DG-538 16x1 Multiplexer

Parts list

2 - DG-538 IC (switches, decoder/latches)
1 - 74HC02 IC (A3 selection)
22 - Supply rail bypass capacitors
16 - PNP transistors (input buffers)
1 - NPN transistor (output level shifter)
50 - Resistors for the above transistors
2 - 16 way connectors (video inputs and grounds)
1 - 6 way connector (address, enable, video out)
1 - 4 way connector (power)
1 - PCB (4" x 5")

Total parts count = 97

THE SILICONIX DG-540 SOLUTION

The DG-540 is configured as four independent analog switches (quad SPST) and has improved frequency performance specifications over the DG-536 and DG-538 due to reduced capacitances and channel ON resistances.

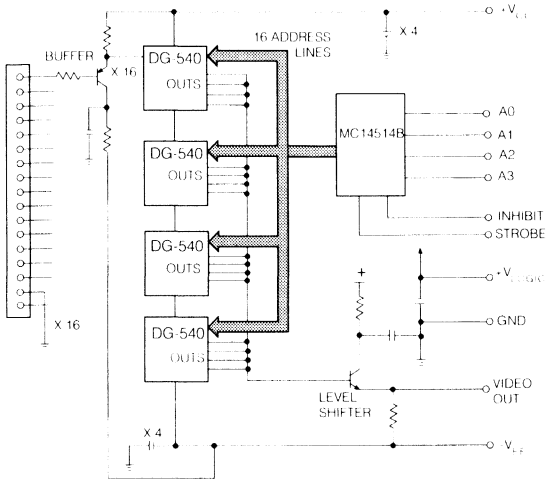


Fig. 4 Circuit Diagram of a DG-540 16x1 Multiplexer

As with the two other devices, the DG-540 requires input transistor buffers. Also, since the device is made up of independent switches with no address decoding nor chip enable function, these have to be provided by external logic. Fortunately, a single 4 to 16 encoder such as the Motorola MC14514B, will perform the Address Selection, Enable and Strobe functions. This device is a 24 pin DIP and occupies a fair amount of PCB real estate. This combined with the area needed for the sixteen input buffers, makes the size of the multiplexer board similar to that of the DG-536 and DG-538.

Parts list

4 - DG-540 IC (switches)
26 - Supply rail bypass capacitors
16 - Transistors (input buffers)
1 - NPN transistor (output level shifter)
50 - Resistors for the above transistors
1 - MC14514B IC (decoder/ latch)
2 - 16 way connectors (video inputs and grounds)
1 - 6 way connector (address/ video out/ enable)
1 - 4 way connector (power)
1 - PCB - (5" by 4")

Total parts count = 102

CONCLUSIONS

The Gennum GX414 is the only device described which is specifically designed for video crosspoint matrices. Furthermore, only the GX414 data sheets specify differential gain and phase, two extremely important video parameters.

The GX414 is the only crosspoint using bipolar switches having unidirectional signal paths and make-before-break switching. These features mean that switching transients are extremely small and that there is virtually no feedback of these onto the input bus. Thus, no external input buffer stages are needed. The bipolar low impedance signal path also means that for high impedance loads (such as the output buffer stage), insertion loss is typically less than 0.035 dB.

At first glance it may appear as though the more complex internal circuitry of the DCMOS devices would have a simpler design solution. However, on comparing system component counts for the four circuits, it is evident that this is not the case.

The following table highlights the significant advantage offered by the Gennum GX414 solution in designing a 16x1 video crosspoint multiplexer.

Solution	Component Count	PCB Area SQ. IN.	Power Consumption (MW)
GX414	20	10	186*
DG536	93	20	242‡
DG538	97	20	304*
DG540	102	20	313*

* V_{CC} = ±8V, V_{LOGIC} = 5 V, T_A = 25°C
(one crosspoint selected, all buffers on I_L = 1 mA)
‡ V_{CC} = +12 V, V_{EE} = -3 V

Engineers at Gennum are always willing to assist the video design engineer in achieving a high performance, cost effective solution to their video routing and switching requirements.

GENNUM CORPORATION

Measuring Up To Broadcast (Differential Gain and Phase)

by John Francis and Paul Moore, Design Engineers, Video/Broadcast Products

INFORMATION NOTE

INTRODUCTION

Measuring non-linearities in video switching systems can be a demanding task when using standard test signal and oscillographic techniques. While it may be possible to measure the relatively large system distortions in this manner, measurement of differential gain (dg) and differential phase (dp) in the smallest system component, the video switch IC, calls for more precise and accurate methods.

In creating a line of video switch products, we have found it necessary to develop improved resolution dg and dp measurement techniques which yield better than 0.001% and 0.001 degrees accuracy. This measurement expertise allows us to minimize crosspoint distortion through optimization of circuit design and application methodology

THE TEST SIGNAL

IEEE Std 206 defines differential gain and phase as the change in magnitude and phase of a small amplitude, high frequency sine wave summed with a low frequency signal changing between two stated levels. As it relates to a composite color television system, differential gain and phase are measured for 20 IRE units of color subcarrier superimposed on a luminance signal which varies from blanking level (0 IRE) to white level (100 IRE).

For AC coupled systems, the average picture level (APL) should be maintained at 10%, 50%, or 90% to ensure that the full range of average operating conditions are observed. Also, a time-varying luminance signal of near 15kHz is usually used as the low frequency component.

For DC coupled systems, the APL does not affect the operating point of the circuit under test and hence is not significant. Further, a well-defined DC luminance component can be used if it is assumed that the DC response of the crosspoint is equivalent to its low frequency response. This is a valid assumption for the wideband video crosspoint. DC conditions simplify the measurement while allowing the use of high resolution test equipment.

To simulate the operating conditions of an AC coupled, composite video system while making a DC coupled measurement, the following table may be used. It shows the required blanking and luminance levels of the test signal for 10%, 50%, and 90% APL in steps of 12.5 IRE units per IEEE Std 206.

DC Coupled		AC Coupled					
APL irrelevant		10% APL		50% APL		90% APL	
Blanking Level (V)	Luminance Level (V)	Blanking Level (V)	Luminance Level (V)	Blanking Level (V)	Luminance Level (V)	Blanking Level (V)	Luminance Level (V)
0	.089	-.029	.060	-.250	-.161	-.464	-.375
0	.179	-.029	.150	-.250	-.071	-.464	-.286
0	.268	-.029	.239	-.250	.018	-.464	-.196
0	.357	-.029	.328	-.250	.107	-.464	-.107
0	.446	-.029	.417	-.250	.196	-.464	-.018
0	.536	-.029	.507	-.250	.286	-.464	.072
0	.625	-.029	.596	-.250	.375	-.464	.161
0	.714	-.029	.685	-.250	.464	-.464	.250

where white level = 100 IRE = 0.714 V (when DC coupled)

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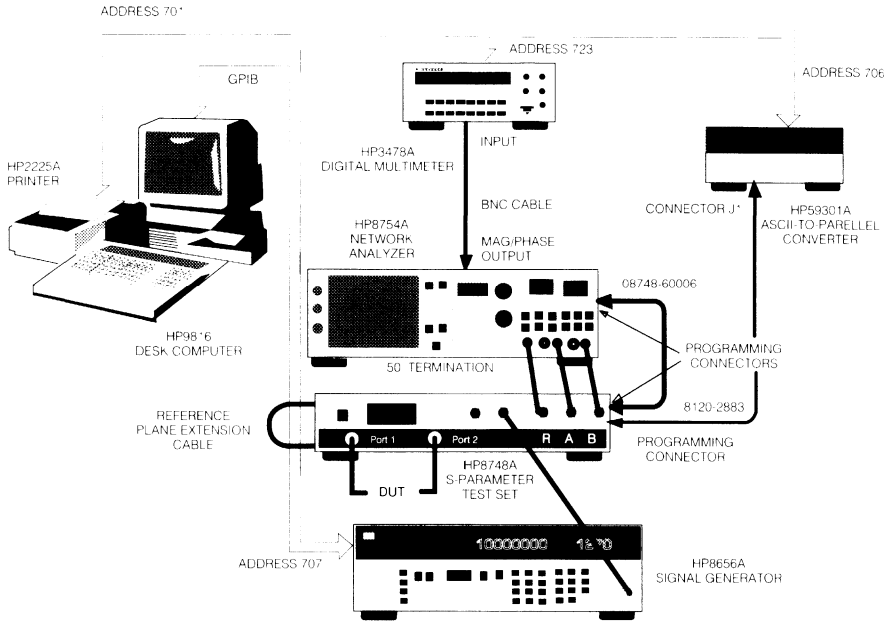

Fig.1 System Block Diagram

MEASUREMENT METHOD

The test equipment used to measure dg and dp is shown in Figure 1.
It consists of :

HP8754A	Network Analyzer
HP 8748A	S-parameter Test Set
HP8656A	Signal Generator
HP3478A	Digital Multimeter
HP59301A	ASCII-to-Parallel Converter
HP9816	Computer
HP2225A	Think Jet Printer

The signal generator is programmed to provide a stable and accurate color subcarrier of user-definable frequency and amplitude. This reference signal is applied to the input of the S-parameter test set and thereby to the device under test (DUT) through port 1 (signal R). The output from the DUT is sampled at port 2 of the S-parameter test set (signal B). The forward transfer characteristic (S21 = B/R) is passed to the network analyzer where the magnitude and phase are measured. A DVM allows the 9816 computer to read the measurement over the General Purpose Interface Bus (GPIB).

As shown in Figure 2, software running on the 9816 computer leads the user through the measurement routine while controlling the test equipment over the GPIB. The computer prompts the user to specify:-

a) gain or phase measurement
b) frequency and amplitude of the subcarrier, and
c) blanking and luminance levels.

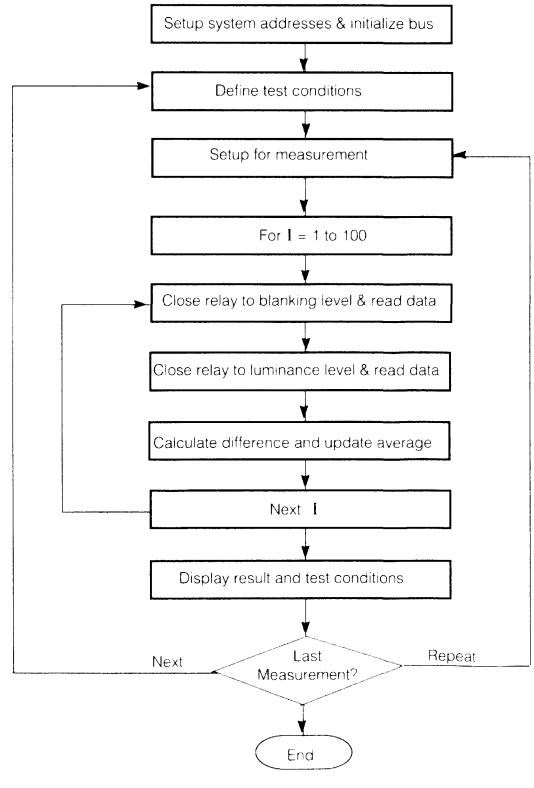

Fig. 2 Flow Chart of Differential Gain and Phase Measurement Program.

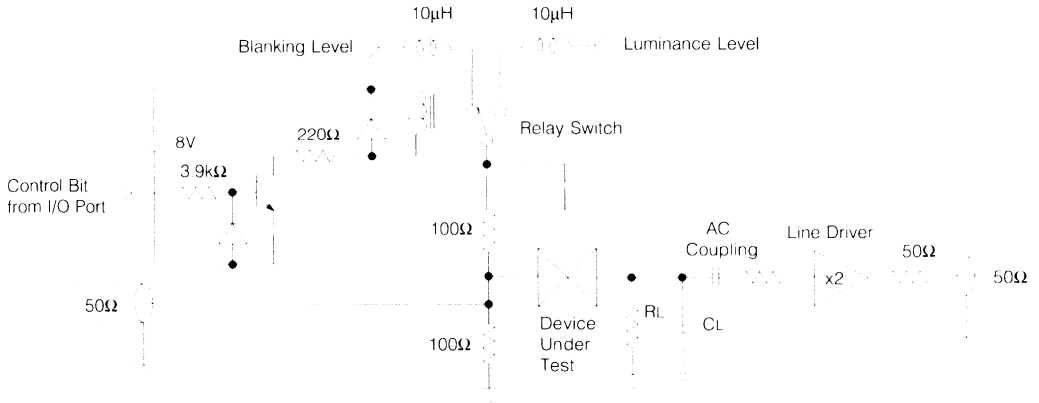

Fig. 3 Simplified Test Circuit

The test circuit of Figure 3 allows two DC bias levels, set by the user, to be superimposed on the color subcarrier from port 1 of the S-parameter test set. A relay,controlled by the 9816 computer, selects either the preset blanking or luminance level. The program takes one measurement at each level and calculates the change in gain or phase of S21. This procedure is repeated one hundred times to provide a reasonably large sample. The results are averaged to reduce the standard deviation and therefore improve the accuracy of the measurement.

The output from the device under test is AC coupled to a buffer amplifier which drives the 50Ω line to port 2 of the S-parameter test set. AC coupling allows the buffer to operate at a constant luminance level so that it does not contribute any dg or dp to the measurement.

MEASUREMENT ACCURACY

The accuracy of the measurement is dependant on :

a) the constancy of the subcarrier signal
b) noise
c) temperature drift.

Since dg and dp are relative measurements, the absolute gain and phase of the forward transfer characteristic (S21) are irrelevant. However, any change in gain or phase not resulting from a change in the luminance level constitutes an error.

Two methods can be used to assess the accuracy of dg / dp measurements:

In the first method, a shorting link is connected in place of the device under test. A typical measurement of dg and dp for this configuration is 0.0002% and 0.0006 degrees. The change in source impedance between coupling the blanking and luminance levels to the input contributes most of this error.

In the second, disconnecting the control to the relay places the device under test at a constant DC bias. Measurements performed on this configuration should give zero dg and dp; in fact, the results are less than 0.0001% for dg and 0.0001 degrees for dp.

These checks ensure that:

a) error from noise is made insignificant by averaging the measurements
b) drift problems do not contribute significant errors.

The important result of this exercise is that the typical GX414 data sheet specifications for dg and dp of 0.03% and 0.012 degrees are not our imagination but can be verified through measurement!

Virtually *Glitch-free* Bipolar Crosspoint Switches

by J. Ian Ridpath and Paul Moore, Design Engineers, Video & Broadcast Products

INFORMATION NOTE

INTRODUCTION

Bipolar video crosspoint switches manufactured by Gennum Corporation are virtually *glitch-free* when compared to switches using CMOS and DMOS technologies.

The reason?

Gennum designed a make-before-break switching circuit to keep the output switching transients small. In addition, the bipolar, unidirectional transmission path offers extremely high output to input signal isolation.

MOS BREAK-BEFORE-MAKE SWITCHING

Both CMOS and DMOS switching are accomplished by altering the channel resistance of the switching transistors from a high impedance off-state to a low impedance on-state. The on-state, (whether or not the switch is configured as a 'T') allows bidirectional transmission of signals from the input to output as well as output to input.

When switching to a second channel, a dead-time must be incorporated to ensure that both channels are not on at the same time. If they are, the two inputs would be effectively shorted together by the on-channel resistances. This break-before-make switching action causes severe *glitches* on the output which are in part coupled to the input by the bidirectional transmission path.

BIPOLAR MAKE-BEFORE-BREAK SWITCHING

In bipolar crosspoints, the output to the input isolation in the enabled or on-state is typically in excess of 85 dB. A series of emitter followers and level shifting diodes produce a transmission path which is inherently unidirectional. Turning on two crosspoints at once results in the signals mixing at the output but interferes little with the input signals. This allows the use of make-before-break switching which keeps the output transient very small.

COMPARISON OF TRANSIENTS BETWEEN CMOS, DMOS AND BIPOLAR SWITCHES

The test set-up to compare the switching transients of a buffered MOS, a T-configured MOS and Gennum's bipolar GX414 monolithic crosspoint is shown in Figure 1.

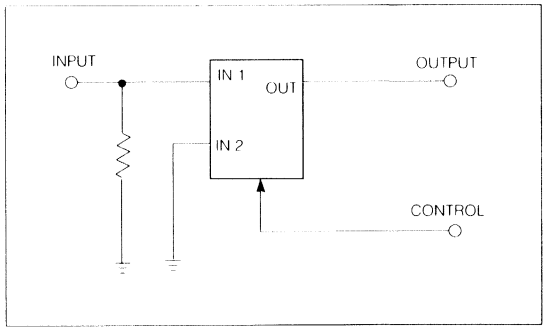

Figure 1

The signal causes the switches to alternate between Input 1 and Input 2. IN 1 is tied to ground by a 75 Ω resistor so that the voltage on it can be monitored by an oscilloscope, while IN 2 is tied directly to ground.

Figures 2, 3 and 4 show the results of these tests. The left hand side of each of these figures show IN 1 and output waveforms when the switch is toggled from IN 1 to IN 2. The right hand side shows the same points when the switch is toggled back from IN 2 to IN 1.

In the buffered CMOS example of Figure 2, an output *glitch* appears which exceeds 250 mV in both the positive and negative direction and a reflected input *glitch* of approximately 10 mV. This output transient is reflected back to the input because the channel is still ON for a short period of time. When switching back from IN 2 to IN 1 the input *glitch* is smaller, since the channel from IN 1 to the output is not yet made. The duration of the input *glitch* is approximately 20 ns, while the output transient rings for an additional 100 ns.

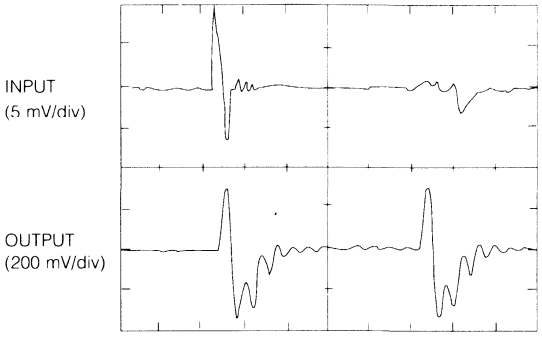

Fig. 2 T-Buffered CMOS (50 ns/div)

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Figure 3 shows that under similar switching conditions, the T-configured DMOS device has a large negative transient of over 100 mV at the input when switched from channel 1 to channel 2, and a smaller positive transient when the device is toggled back. The large negative pulse at the output represents the dead-time and clearly shows the break-before-make switching action. However, it should be noted that a large amount of overshoot occurs on the rising edge of the output signal. Again, the duration of the input *glitches* is quite short and varies between 20 ns to 40 ns, while the output dead-time exceeds 70 ns.

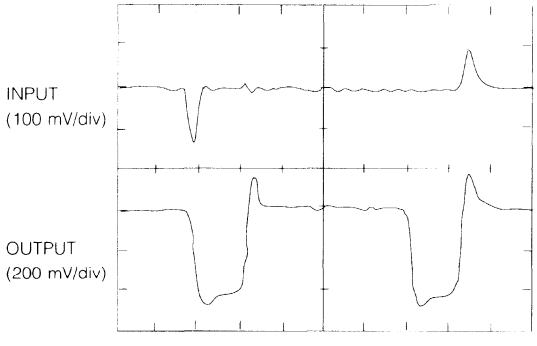


Fig. 3 T-Configured DMOS (50 ns/div)

The last figure shows the minimal transients produced by the bipolar crosspoint. Note the change in scales for both the amplitude and time duration. The input *glitches* are not due to the output transients, but are a function of the bias current on the input emitter follower transistor. The negative going output transient is less than 20 mV peak, and has a duration of approximately 100 ns. It is followed by a damped waveform of less than 20 mV peak, having a fundamental period of about 600 ns. These low frequency transients do not create any out-of-band noise and do not need to be filtered.

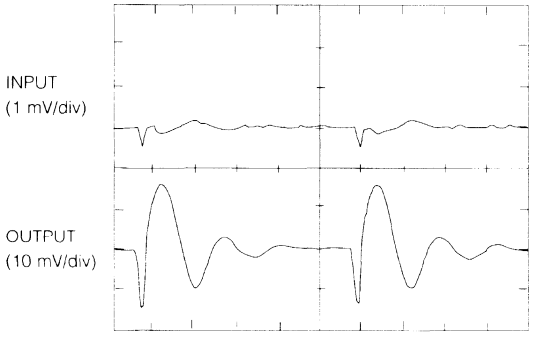


Fig.4 GX414 Bipolar (500 ns/div)

CONCLUSIONS

For MOS switches to be used as video crosspoints, extra external circuitry is always needed. The external circuitry usually consists of input buffers (having very low output impedance) and an output clamping circuit.

In DMOS circuits, the input buffer (which is usually an emitter follower) is used to provide isolation from the switching transients present at the input of each switch. If the buffer was not included and multi-inputs were used in a matrix configuration, *glitches* would appear on the input bus and affect all other crosspoints connected to that bus. Gennum's GX414, GX414A, GX424 and GX434 bipolar crosspoints have that buffer built-in.

The ratio of ON to OFF capacitance at the input of a MOS switch can be an order of magnitude or more. The absolute capacitance could change from 4 pF to 45 pF. This means the input drive signal sees an undesireable, widely changing impedance. With the built-in buffer the Gennum products listed have an input ON to OFF capacitance ratio near unity, with absolute values of only 2.0 pF and 2.4 pF.

The serious output *glitches* produced by the MOS switches could be interpreted as sync pulses by subsequent equipment. To remove this problem, the output must be clamped during the switching dead-time. The output transients generated by Gennum crosspoints are extremely small and clamping is not needed.

Even though MOS crosspoint switches consume less power, the saving is negated by the external circuitry necessary to make the switch function properly in a video system. Gennum's family of bipolar crosspoints require no extra circuitry since they are designed specifically for video routing and switching applications.

RESONANT MODE CONTROLLERS

RMD
data sheets

RMA
application notes

GENNUM CORPORATION

Resonant Mode Power Supply Controller

GP605 DATA SHEET

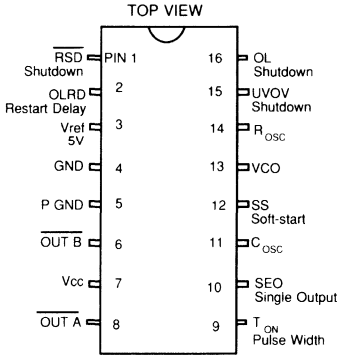
RMD 1

FEATURES

* frequency range of 1 kHz to 2 MHz
* operating frequency range (min. and max.) set by a resistor and a capacitor
* pulse width set by a resistor and capacitor
* synchronous overload shutdown with delayed restart
* synchronous overvoltage, undervoltage and remote shutdown
* soft-start
* single-ended or complementary outputs
* drives power MOSFETs directly (0.8A peak)
* low cost 16 pin DIP or SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	20V
Undervoltage/Overvoltage Input	-0.4V - 6V
Overload Input	-0.4V - 6V
Remote Shutdown	-0.4V - Vcc
VCO Input	-0.4V - Vcc
Storage Temperature	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec)	260°C
Junction Temperature	150°C
Power dissipation at T_A ≤ 70°C (derate 9 mW/°C for T_A > 70°C)	720 mW



PIN CONNECTION
16 PIN DIP

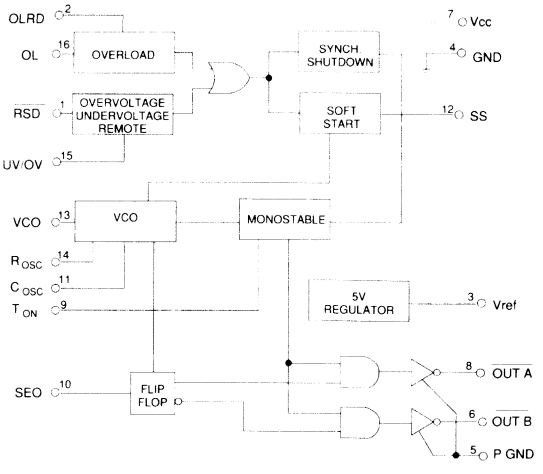
CIRCUIT DESCRIPTION

The GP605 utilizes frequency modulation instead of pulse width modulation to achieve regulation. The pulse width is held constant while the frequency is varied over an operating range set by a resistor and capacitor. A feedback voltage controls the switching frequency of the two complementary outputs, which are capable of driving power MOSFETs directly.

Opening a normally grounded control pin puts the GP605 into single-ended operation. In this mode the frequency is doubled and the two outputs are identical so they can be paralleled for increased drive capability.

The high operating frequency of up to 2 MHz results in significant reductions in the size of the required magnetic and capacitive components in the power supply. This leads to dramatic savings in volume, weight and manufacturing cost of switching power supplies.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed.



FUNCTIONAL BLOCK DIAGRAM

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ELECTRICAL CHARACTERISTICS

Limits apply over $0°C \leq T_A \leq 70°C$ for the GP605CD and GP605CK,
$-25°C \leq T_A \leq 85°C$ for the GP605ID and GP605IK, and
$-55°C \leq T_A \leq 125°C$ for the GP605M

Parameters tested on open loop test circuit
Typical values are at $T_A = 25°C$
* Parameters marked with an asterisk* are valid only at $T_A = 25°C$
$V_{CC} = 12V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Internal Vcc Undervoltage Threshold		8.5	9.0	9.5	V
Threshold Hysteresis		-	5	-	%
Supply Current	Undervoltage condition	18	22	24	mA
Voltage Control Oscillator					
Maximum Frequency	Single output Complementary output	- -	2 1	- -	MHz MHz
Tolerance of f max Tolerance of f min	Fig. 6 Fig. 5	- -	- -	±5 ±20	% %
Temperature coefficient $f$max Temperature coefficient $f$min		-300 400	-600 700	-900 1000	ppm/°C ppm/°C
Dead Time T_{OFF}*		-	200	300	ns
Operating Range of VCO Input (Pin 13)	max min	- -	6.5 1.1	- -	V V
Linearity of the VCO		-	-	±5	%
Internal Pull-up Resistor (Pin 13)		8	10	12	kΩ
Output Pulse Width T_{ON} Tolerance		-	-	±5	%
Temperature Coefficient of T_{ON}		0	400	800	ppm/°C
Output Section					
Output Risetime Output Falltime	100pF II 100kΩ load on $\overline{OUT\ A}$, $\overline{OUT\ B}$	- -	20 15	40 30	n sec n sec
Output Mismatch	$\overline{OUT\ A}$ & $\overline{OUT\ B}$, Pin 10 SEO open	-	5	25	n sec
Output Low Level (sink)	$\overline{OUT\ A}$ vs $\overline{OUT\ B}$ 20mA 200mA	- -	- -	0.7 2.7	V V
Output High Level (source)	$\overline{OUT\ A}$ & $\overline{OUT\ B}$ -20mA -200mA	V_{CC} -2.5 V_{CC} -2.8	- -	- -	V V
Reference Section					
Output Voltage*		4.75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Max Current Capability		-	10	-	mA

ELECTRICAL CHARACTERISTICS continued

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Section					
Soft-start (1)	C_S = 2.2 µF, VCO = 7V	16	19	22	ms
Overload Restart Delay	2R = 330 kΩ, C = 6.8 µF	1.0	1.3	1.6	sec
Propagation Delay to Shutdown (2)		-	200	300	n sec
Remote Shutdown (3)	Enabled	Vcc -0.8	-	-	V
	Disabled	-	-	3	V
Overload Shutdown (OL) Threshold*		2.84	3.0	3.16	V
OL Threshold Temp. Coefficient		-400	100	500	ppm/°C
OL Hysteresis		-	3	-	%
OL Trigger Pulse Width		500	-	-	n sec
OL Input current Range		-1	-	+15	µA
Overvoltage Threshold* Lockout		2.84	3.0	3.16	V
Undervoltage Threshold* Lockout		1.8	1.9	2	V
Temp. Coeff. of Thresh'd Voltage		-400	100	500	ppm/°C
Hysteresis of the Lockout Voltage		-	3	-	%
Input Current Range (Pin 15)		-1	-	+22	µA
Thermal Impedance	16 pin DIL Plastic Package θ JC	-	42	-	°C/W
	16 pin DIL Plastic Package θ CA	-	70	-	°C/W
	16 Pin SOIC θ JA	_	112	-	°C/W

NOTE

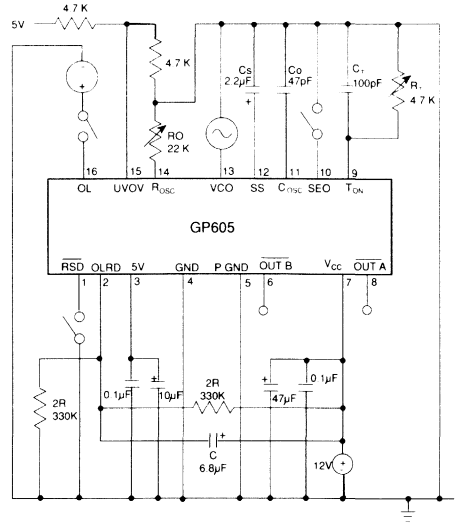
(1) Soft-start time is measured from output enable at minimum frequency to time at which maximum frequency is reached.

(2) If the shutdown input is triggered 200 ns before the next output pulse is expected, there will be no pulses. If there is a pulse earlier than 200 ns, this pulse is completed in full before the output is disabled. This is known as synchronous shutdown, a necessary feature in any resonant mode controller.

(3) Refer to pin description for current required.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GP605CD	16 Pin DIP	0° to 70° C
GP605CK	16 Pin SOIC	0° to70° C
GP605ID	16 Pin DIP	-25° to 85° C
GP605IK	16 Pin SOIC	-25° to 85° C
GP605M	TBD	-55° to 125° C



Open Loop Test Circuit

RMD 1

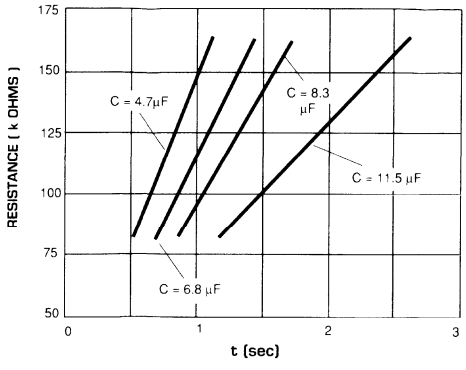


Fig. 1 Overload Restart Delay

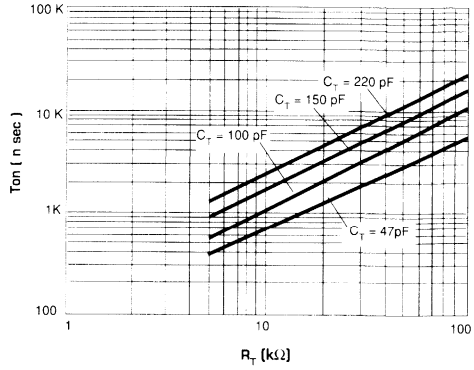


Fig. 2 Output Pulse Width

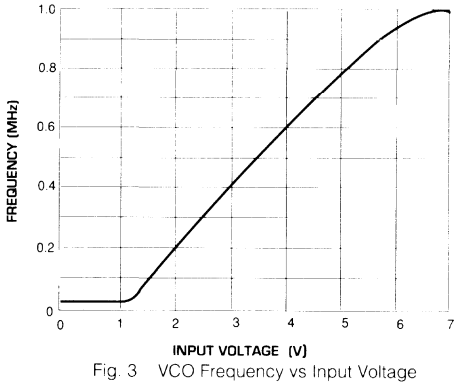


Fig. 3 VCO Frequency vs Input Voltage

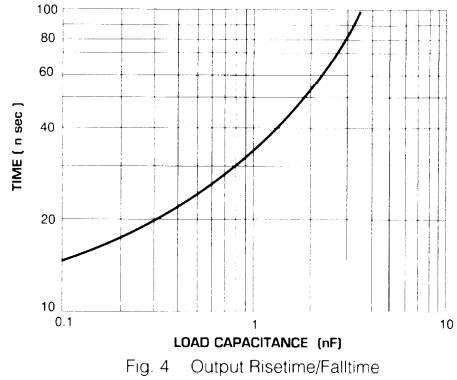


Fig. 4 Output Risetime/Falltime

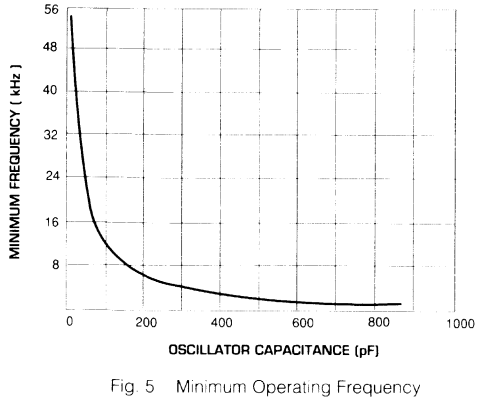


Fig. 5 Minimum Operating Frequency

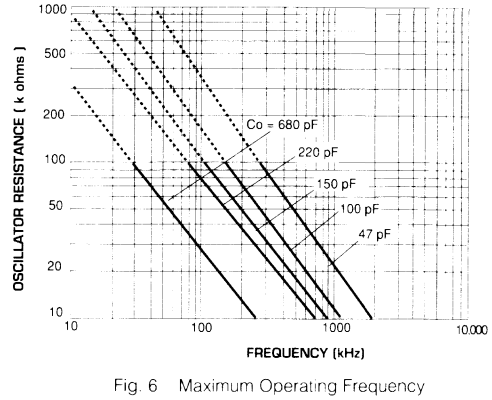


Fig. 6 Maximum Operating Frequency

TYPICAL PERFORMANCE CURVES OF THE GP605

For all graphs, *Vcc* = +12 volts DC and T_A = 25 °C. The curves shown above represent typical batch sampled results.

PIN FUNCTIONS

The GP605 is a complex device, so the best place to start is with a functional pin description.

Pin 1 (*RSD*) - Remote Shutdown
A low on pin 1 shuts down the GP605. When the pin is released the GP605 goes into soft-start. This pin is normally driven by an open collector transistor where the current is given by:

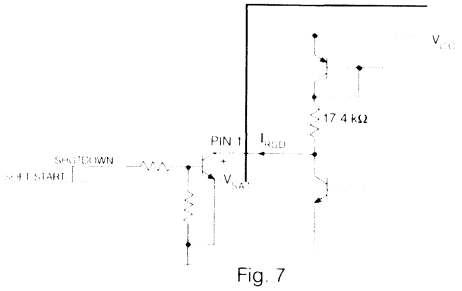


Fig. 7

$$I_{RSD} = \frac{(V_{CC} - V_{SAT} - 0.7)V}{17.4\ k\Omega} \quad mA \pm 20\%$$

For CMOS or bipolar circuitry, the configuration may be:

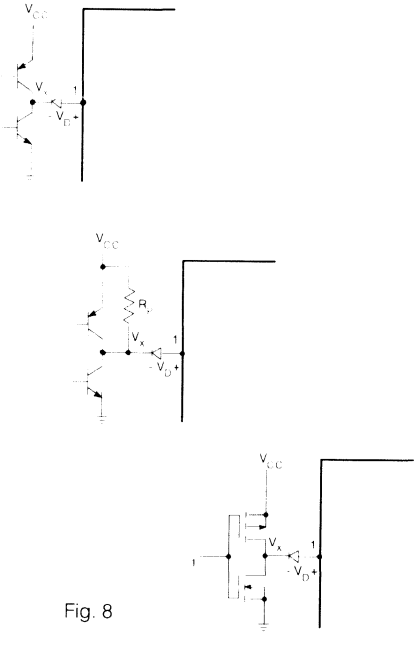


Fig. 8

In all cases the voltage must pull up to a minimum of

$$V_X = V_{CC} - 0.8V$$

assuming diode voltage $V_D \approx 0.4V$ when it is off (non-conducting). If remote shutdown is not used, leave pin 1 open.

Pin 2 (*OLRD*) - Overload Restart Delay
A 330 kΩ + 330 kΩ voltage divider in combination with a 6.8 µF capacitor generates a 1.3 second shutdown to restart delay every time the overload sense (pin 16) is activated. Timing starts when the overload is removed; upon timeout soft-start begins. Refer to Figure 1 to select RC combinations for other delays.

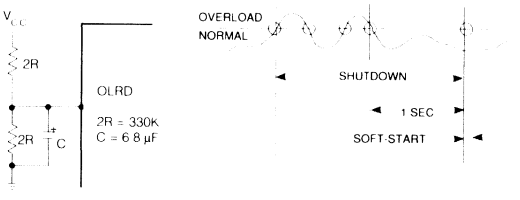


Fig. 9

Pin 3 (*5V*) - 5V Reference
This is a 5% tolerance regulator used to power most of the internal circuitry. To improve noise rejection it is recommended to decouple this pin with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 3 can be used as a reference for any external circuitry as long as the load is less than 10 mA.

Pin 4 (*GND*) - Analog Ground
Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimized and do not interfere with feedback voltages and the reference.

Pin 5 (*P GND*) - Power Ground
Only the output transistors are connected to the power ground, to minimize interference with the logic circuitry.

GND and *P GND* are to be connected outside the package, with the decoupling of the supply to this point.

Pin 6 ($\overline{OUT\ B}$) - Output B
Output B is an active low output driver, where the low duration (pulse width) is T_{ON}. It is complementary to pin 8 ($\overline{OUT\ A}$). For proper operation, the voltage on the output pins must not go below ground potential or above V_{CC} by more than 0.5 volts.

Pin 7 (V_{CC}) - Supply Voltage
The power supply trace must be decoupled as close to pin 7 as possible. Currents of 0.5 A levels may be drawn by the GP605. Minimum recommended decoupling is with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 8 ($\overline{OUT\ A}$) - Output A
Output A is an active low output driver, where the low duration (pulse width) is T_{ON}, and is complementary to pin 6.

Pin 9 (T_{ON}) - Pulse Width

The constant pulse width T_{ON} is set by a resistor R_T and capacitor C_T. This relationship is shown in Figure 2. $R_T \times C_T$ should have a temperature coefficient of -500 ppm/°C for best stability and fall within the following ranges:

$$5\ k\Omega \leq R_T \leq \text{no limit}$$
$$47\ pF \leq C_T \leq 100\ nF$$

The R_T and C_T should be connected as close as possible to *GND* to minimize ground noise variations. The upper limit on pulse width is determined by chip-to-chip variation, power supply and component tolerances. The worst case combination must give $T_{ON} < 1/f\text{max} - T_{OFF}$, where $T_{OFF} = 200$ ns typ. (300 ns max.). The off period is required by the design of the GP605. The pulse width T_{ON} should be set to give an off period greater than T_{OFF} so that the circuit will operate correctly at $f$max, where f is the actual operating frequency. Rewriting the equation as:

$$T_{OFF} = 1/f - T_{ON}$$

The GP605 will divide the output frequency by two when T_{OFF} decreases to 200 ns. This is a failsafe feature to ensure the pulse width will never be incorrect by limiting $f$max. Under normal operation $f$max should be limited using R_{OSC}.

Pin 10 (*SEO*) - Single Ended Output

This pin is normally grounded for complementary outputs in push-pull applications. Opening pin 10 results in a single ended output at double the frequency. $\overline{OUTA}$ and $\overline{OUTB}$ can then be shorted together for increased drive capability.

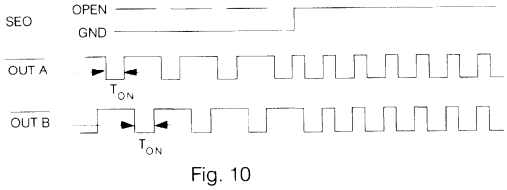


Fig. 10

Pin 11 (C_{OSC}) - Oscillator Capacitor

The capacitor C_{OSC} on this pin, controls the minimum frequency $f$min of the *VCO* operating range. Refer to Figure 5 for selection. Layout is critical for this component, keeping leads as short as possible and connecting close to the *GND* pin.

Pin 12 (*SS*) - Soft-Start

A capacitor C_S on this pin provides a controlled start up from $f$min to $f$max. The delay is approximately $t_{SS}(ms) \approx 8.7\ C_S(\mu F)$ for C_S between zero and 47µF.

To ensure a full soft-start duration when soft-start is caused by an undervoltage or overvoltage fault, it is necessary to have the fault present for about half the soft-start time.

Pin 13 (*VCO*) - Voltage Controlled Oscillator Input

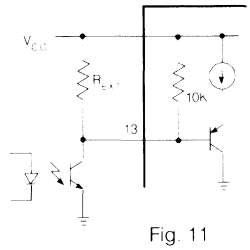


Fig. 11

The VCO input is designed for an optocoupler feedback network from the secondary (output) side of the power supply. An internal 10 kΩ pull-up resistor is provided but an external resistor may be used if a lower value is required. The control characteristic is shown in Figure 3. The linear input range is from 1.1 V to 6.5 V where 1.1 V represents $f$min and 6.5 V represents $f$max.

Pin 14 (R_{OSC}) - Oscillator Resistor

The resistor R_{OSC} on this pin, controls $f$max, the maximum frequency of the *VCO* operating range. C_{OSC} the capacitor controlling $f$min must be selected first, then refer to Figure 6 for selection of R_{OSC}. For good stability, a 1% resistor with a temperature coefficient of -600 ppm/°C, is recommended. Minimum value for R_{OSC} is 10 kΩ.

Pin 15 (*UVOV*) - Undervoltage/Overvoltage

The input is a window comparator. A higher or lower voltage than the thresholds specified will shut down the power supply until voltage falls within the window again, at which point the GP605 goes into soft-start. If pin 15 is not used, it must be tied to V_{CC} or the *5 V* reference via a voltage divider, generating a bias voltage, which falls within the window. The voltage divider should carry approximately 1 mA. The maximum input voltage on this pin is 6 V.

Pin 16 (*OL*) - Overload Input

A voltage exceeding the specified threshold on this pin will cause the GP605 to shut down and activate the overload restart delay function. This delay starts when the input voltage drops below the threshold. On time-out, soft-start begins. The maximum input voltage on this pin is 6 V. If pin 16 is not used, short it to ground. No capacitor is required on pin 2 (*ORLD*), but a bias voltage between $V_{CC}/3$ and $V_{CC}/3 + 5.7$ V is still needed. A convenient voltage is $V_{CC}/2$.

A TYPICAL APPLICATION CONFIGURATION

Figure 7 shows the GP605 as a resonant mode power supply providing 5V DC output. L_r and C_r form the series resonant tank. V_{CC} is generated locally for high efficiency, using a start-up circuit which is biased off after V_{CC} stabilises. *T2* senses the current in the primary of *T3* and provides the overload signal.

For more information, request Application Note 510-62.

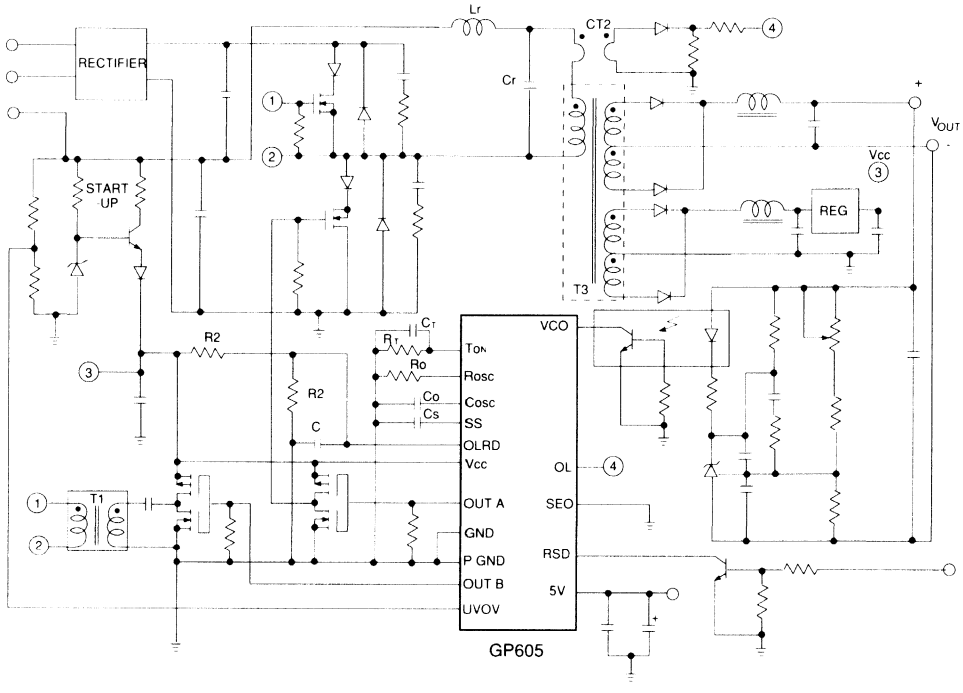


Fig. 12 Typical GP605 Application

AVAILABLE PACKAGING

16 pin DIP or 16 pin SOIC

CAUTION

ELECTROSTATIC

SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

RMD 1

GENNUM CORPORATION

Push - Pull, Resonant Mode Power Supply Controllers

GP6050 and GP6051
PRELIMINARY DATA SHEET

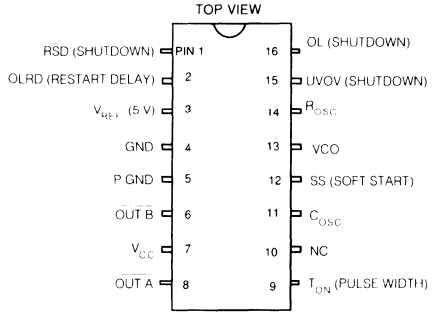
RMD 2

FEATURES

* frequency range of 1 kHz to 3 MHz
* operating frequency range set by a resistor (max.) and a capacitor (min.)
* pulse width set by a resistor and capacitor
* low start-up current
* synchronous overload shutdown with delayed soft restart
* synchronous overvoltage, undervoltage and remote shutdown
* soft-start
* complementary outputs
* drives power MOSFETs directly (0.8A peak)
* low cost 16 pin DIP or SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	20V
Undervoltage/Overvoltage Input	-0.4V - 6V
Overload Input	-0.4V - 6V
Remote Shutdown	-0.4V - Vcc
VCO Input	-0.4V - Vcc
Storage Temperature	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec.)	260°C
Junction Temperature	150°C
Power dissipation at T_A ≤ 70°C (derate 9 mW/°C for T_A > 70°C)	720 mW



PIN CONNECTION
16 PIN DIP

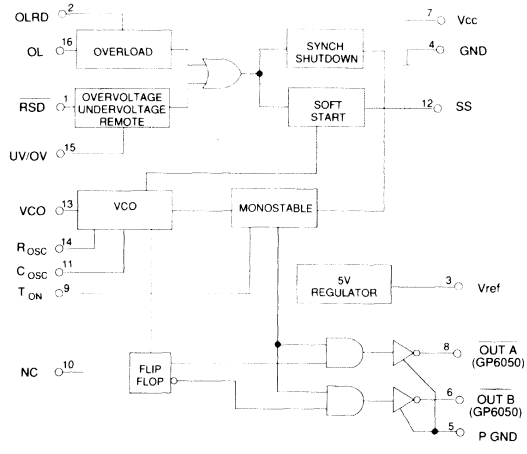
CIRCUIT DESCRIPTION

The GP6050 and GP6051 are highly reliable, complementary output, resonant mode power supply controllers. The GP6050 is an upgraded, pin-to-pin compatible version of the GP605. The GP6051 provides an inverted driver output with respect to the GP6050. These devices support resonant and quasi-resonant topologies operating in variable frequency mode. To achieve regulation the pulse width is held constant while the frequency is varied by a feedback voltage over an operating range. Maximum and minimum frequency is set by an external resistor and capacitor. Fixed pulse width is adjusted by an external RC network.

The complementary totem pole outputs have 0.8 A peak current capability. The GP6050 provides active low driver output. The GP6051 provides active high driver output.

The high operating frequency of up to 3 MHz results in significant reductions in EMI noise and minimizes the size of the required magnetic and capacitive components in the power supply.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed. The controller also contains power supply undervoltage lockout, minimizing supply current during the start-up condition.

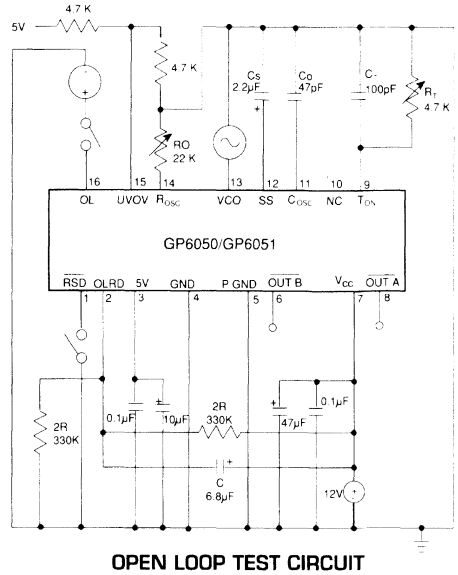


FUNCTIONAL BLOCK DIAGRAM

Document No. 510 - 58 - 1

Part Number	Package Type	Temperature Range
GP6050 CD GP6051 CD	16 Pin DIP	0° to 70° C
GP6050 CK GP6051 CK	16 Pin SOIC	0° to70° C
GP6050 ID GP6051 ID	16 Pin DIP	-25° to 85° C
GP6050 IK GP6051 IK	16 Pin SOIC	-25° to 85° C
GP6050 M GP6051 M	TBD	-55° to 125° C

ORDERING INFORMATION



OPEN LOOP TEST CIRCUIT

ELECTRICAL CHARACTERISTICS

Limits apply over
$0°C \le T_A \le 70°C$ for the GP6050/51CD, andGP6050/51CK
$-25°C \le T_A \le 85°C$ for the GP6050/51ID and GP6050/51IK
$-55°C \le T_A \le 125°C$ for the GP6050/51M

Parameters tested on open loop test circuit
Typical values are at $T_A = 25°C$
* Parameters marked with an asterisk* are valid only at $T_A = 25°$
$V_{CC} = 12V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Chip Enable V_{CC} Threshold		11.3	12	12.7	V
V_{CC} Under Voltage Lockout		8.5	9.0	9.5	V
Supply Current	Undervoltage condition Normal condition	- 18	5 22	- 24	mA mA
Voltage Control Oscillator					
Maximum Frequency	Single output Complementary output	2.4 1.2	3 1.5	- -	MHz MHz
Tolerance of $f$max Tolerance of f min	Fig. 6 Fig. 5	- -	- -	±5 ±20	% %
Temperature coefficient $f$max Temperature coefficient $f$min		-300 400	-600 700	-900 1000	ppm/°C ppm/°C
Dead Time T_{OFF}*		-	100	125	ns
Operating Range of VCO Input (Pin 13)	max min	- -	6.5 1.1	- -	V V
Linearity of the VCO		-	-	±5	%
Internal Pull-up Resistor (Pin 13)		8	10	12	kΩ
Output Pulse Width T_{ON} Tolerance		-	-	±5	%
Temperature Coefficient of T_{ON}		0	400	800	ppm/°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Risetime	100pF II 100kΩ load on	-	20	40	n sec
Output Falltime	$\overline{OUT}$ A, OUT B	-	15	30	n sec
Output Mismatch	$\overline{OUT}$ A & $\overline{OUT}$ B , Pin 10 SEO open	-	5	15	n sec
Output Low Level (sink)	$\overline{OUT}$ A vs $\overline{OUT}$ B 20mA	-	-	0.7	V
	200mA	-	-	2.2	V
Output High Level (source)	$\overline{OUT}$ A & $\overline{OUT}$ B -20mA	-	-	Vcc -2	V
	-200mA	-	-	Vcc -2.2	V
Reference Section					
Output Voltage*		4.75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Max Current Capability		-	10	-	mA
Shutdown Section					
Soft-start (1)	C_S = 2.2 µF, VCO = 7V	16	19	22	ms
Overload Restart Delay	2R = 330 kΩ, C = 6.8 µF	1.0	1.3	1.6	sec
Propogation Delay to Shutdown (3)		-	200	300	n sec
Remote Shutdown (2)	Enabled	Vcc -0.8	-	-	V
	Disabled	-	-	3	V
Overload Shutdown (OL) Threshold*		2.84	3.0	3.16	V
OL Threshold Temp. Coefficient		-400	100	500	ppm/°C
OL Hystersis		-	3	-	%
OL Trigger Pulse Width		500	-	-	n sec
OL Input current Range		-1	-	+15	µA
Overvoltage Threshold* Lockout		2.84	3.0	3.16	V
Undervoltage Threshold* Lockout		1.8	1.9	2.0	V
Temp. Coeff. of Thresh'd Voltage		-400	100	500	ppm/°C
Hystersis of the Lockout Voltage		-	3	-	%
Input Current Range (Pin 15)		-1	-	+22	µA
Thermal Impedance	16 pin DIL Plastic Package θ JC	-	42	-	°C/W
	16 pin DIL Plastic Package θ CA	-	70	-	°C/W
	16 Pin SOIC θ JA	-	112	-	°C/W

NOTES

(1) Soft-start time is measured from output enable at minimum frequency to time at which maximum frequency is reached.

(2) Refer to pin description for current required.

(3) If the shutdown input is triggered 200 ns before the next output pulse is expected, there will be no pulses. If there is a pulse earlier than 200 ns, this pulse is completed in full before the output is disabled. This is known as synchronous shutdown, a necessary feature in any resonant mode controller.

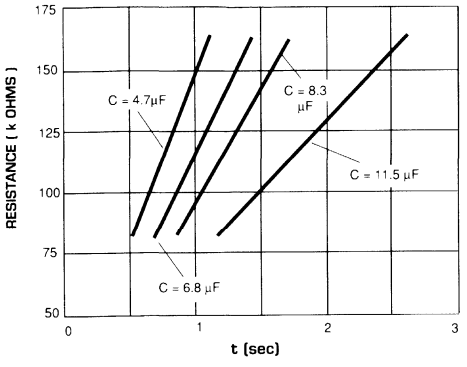


Fig. 1 Overload Restart Delay

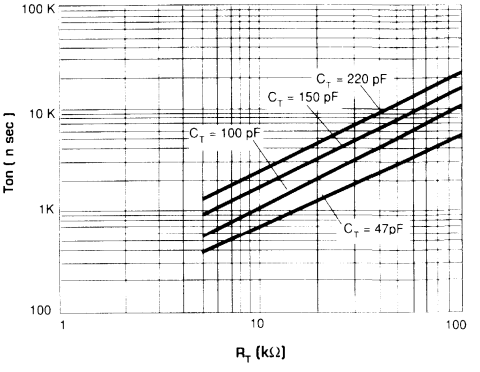


Fig. 2 Output Pulse Width

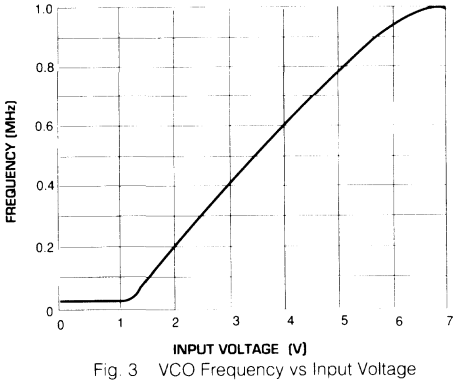


Fig. 3 VCO Frequency vs Input Voltage

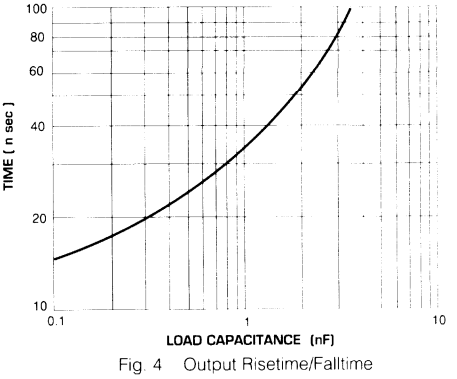


Fig. 4 Output Risetime/Falltime

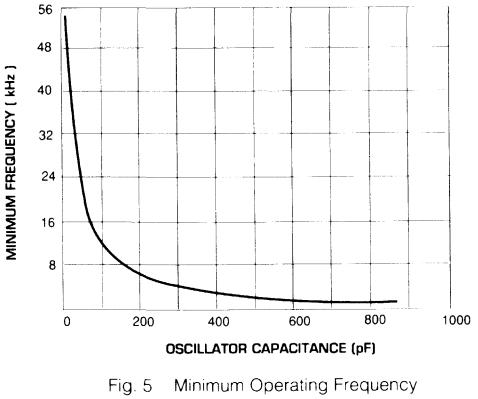


Fig. 5 Minimum Operating Frequency

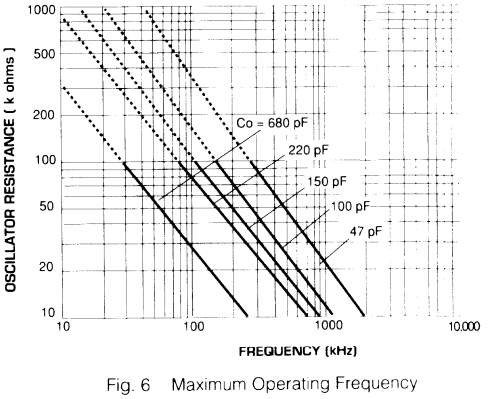


Fig. 6 Maximum Operating Frequency

TYPICAL PERFORMANCE CURVES OF THE GP6050 AND GP6051

For all graphs, *Vcc* = +12 volts DC and T_A = 25 °C. The curves shown above represent typical batch sampled results.

PIN FUNCTIONS

The GP6050 and GP6051 are complex devices, so the best place to start is with a functional pin description.

Pin 1 (*RSD*) - Remote Shutdown
A low on pin 1 shuts down the GP6050 or GP6051. When the pin is released the controller goes into soft-start. This pin is normally driven by an open collector transistor where the current is given by:

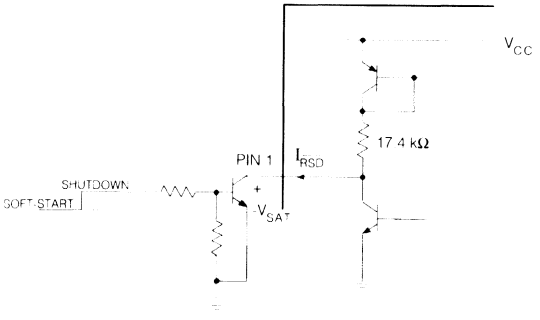


Fig. 7

$$I_{\overline{RSD}} = \frac{(V_{CC} - V_{SAT} - 0.7)V}{17.4\ k\Omega} \quad mA \pm 20\%$$

For CMOS or bipolar circuitry, the configuration may be:

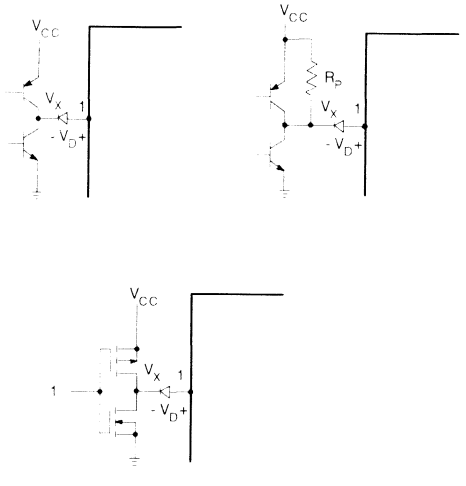


Fig. 8

In all cases the voltage must pull up to a minimum of

$$V_X = V_{CC} - 0.8V$$

assuming diode voltage $V_D \approx 0.4V$ when it is off (non-conducting). If remote shutdown is not used, leave pin 1 open.

Pin 2 (*OLRD*) - Overload Restart Delay
A 330 kΩ + 330 kΩ voltage divider in combination with a 6.8 µF capacitor generates a 1.3 second shutdown to restart delay every time the overload sense (pin 16) is activated. Timing starts when the overload is removed; upon timeout soft-start begins. Refer to Figure 1 to select RC combinations for other delays.

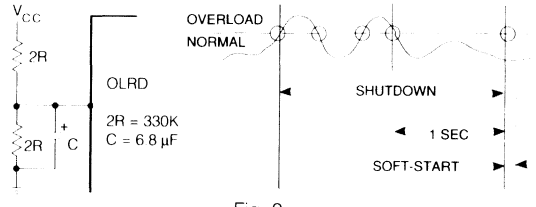


Fig. 9

Pin 3 (*5V*) - 5V Reference
This is a 5% tolerance regulator used to power most of the internal circuitry. To improve noise rejection it is recommended to decouple this pin with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 3 can be used as a reference for any external circuitry as long as the load is less than 10 mA.

Pin 4 (*GND*) - Analog Ground
Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimized and do not interfere with feedback voltages and the reference.

Pin 5 (*P GND*) - Power Ground
Only the output transistors are connected to the power ground, to minimize interference with the logic circuitry.

GND and *P GND* are to be connected outside the package, with the decoupling of the supply to this point.

Pin 6 (*OUT B*) - Output B
The GP6050 provides on output B, an active low during fixed pulse width. The GP6051 provides on output B, an active high during fixed pulse width. Output B is complementary to output A (pin 8). For proper operation, the voltage on the output pins must not go below ground potential or above V_{CC} by more than 0.5 V.

Pin 7 (V_{CC}) - Supply Voltage
The power supply trace must be decoupled as close to pin 7 as possible. Currents of 0.5 A levels may be drawn by the controller. Minimum recommended decoupling is with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 8 (*OUT A*) - Output A
The GP6050 provides on output A, an active low during fixed pulse width. The GP6051 provides on output A, an active high during fixed pulse width. Output A is complementary to output B (pin 6).

Pin 9 (T_{ON}) - Pulse Width

The fixed pulse width T_{ON} is set by a resistor R_T and capacitor C_T. This relationship is shown in Figure 2. $R_T \times C_T$ should have a temperature coefficient of -500 ppm/°C for best stability and fall within the following ranges:

$$5\ k\Omega \leq R_T \leq \text{no limit}$$
$$47\ pF \leq C_T \leq 100\ nF$$

The R_T and C_T should be connected as close as possible to *GND* to minimize ground noise variations. The upper limit on pulse width is determined by chip-to-chip variation, power supply and component tolerances. The worst case combination must give $T_{ON} < 1/f\text{max} - T_{OFF}$, where $T_{OFF} = 100$ ns typ. (125 ns max.). The off period is required by the design of the GP605. The pulse width T_{ON} should be set to give an off period greater than T_{OFF} so that the circuit will operate correctly at $f$max, where f is the actual operating frequency. Rewriting the equation as:

$$T_{OFF} = 1/f - T_{ON}$$

The controller will divide the output frequency by two when T_{OFF} decreases to 100 ns. This is a failsafe feature to ensure the pulse width will never be incorrect by limiting $f$max. Under normal operation $f$max should be limited using R_{OSC}.

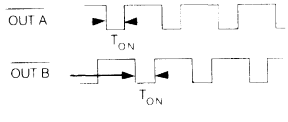


Fig. 10

Pin 10 - NC

Pin 11 (C_{OSC}) - Oscillator Capacitor

The capacitor C_{OSC} on this pin, controls the minimum frequency $f$min of the *VCO* operating range. Refer to Figure 5 for selection. Layout is critical for this component, keeping leads as short as possible and connecting close to the *GND* pin.

Pin 12 (*SS*) - Soft-Start

A capacitor C_S on this pin provides a controlled start up from $f$min to $f$max. The delay is approximately $t_{SS}(\text{ms}) \approx 8.7\ C_S(\mu\text{F})$ for C_S between zero and 47µF.

To ensure a full soft-start duration when soft-start is caused by an undervoltage or overvoltage fault, it is necessary to have the fault present for about half the soft-start time.

Pin 13 (*VCO*) - Voltage Controlled Oscillator Input

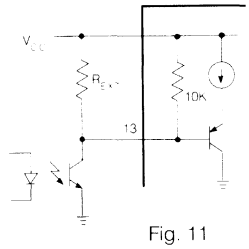


Fig. 11

The VCO input is designed for an optocoupler feedback network from the secondary (output) side of the power supply. An internal 10 kΩ pull-up resistor is provided but an external resistor may be used if a lower value is required. The control characteristic is shown in Figure 3. The linear input range is from 1.1 V to 6.5 V where 1.1 V represents $f$min and 6.5 V represents $f$max.

Pin 14 (R_{OSC}) - Oscillator Resistor

The resistor R_{OSC} on this pin, controls $f$max, the maximum frequency of the *VCO* operating range. C_{OSC} the capacitor controlling $f$min must be selected first, then refer to Figure 6 for selection of R_{OSC}. For good stability, a 1% resistor with a temperature coefficient of -600 ppm/°C, is recommended. Minimum value for R_{OSC} is 10 kΩ.

Pin 15 (*UVOV*) - Undervoltage/Overvoltage

The input is a window comparator. A higher or lower voltage than the thresholds specified will shut down the power supply until voltage falls within the window again, at which point the controller goes into soft-start. If pin 15 is not used, it must be tied to V_{CC} or the *5V* reference via a voltage divider, generating a bias voltage, which falls within the window. The voltage divider should carry approximately 1 mA. The maximum input voltage on this pin is 6V.

Pin 16 (*OL*) - Overload Input

A voltage exceeding the specified threshold on this pin will cause the controller to shut down and activate the overload restart delay function. This delay starts when the input voltage drops below the threshold. On time-out, soft-start begins. The maximum input voltage on this pin is 6V. If pin 16 is not used, short it to ground. No capacitor is required on pin 2 (*ORLD*), but a bias voltage between $V_{CC}/3$ and $V_{CC}/3 + 5.7$ V is still needed. A convenient voltage is $V_{CC}/2$.

A TYPICAL APPLICATION CONFIGURATION

Figure 7 shows the GP6050 as a resonant mode power supply providing 5V DC output. Capacitors C_r in series with inductor L_r form the resonant tank. The load transformer *T1* is attached in parallel to resonant tank capacitors. For more information, request parallel resonant mode converter Application Note 510-62

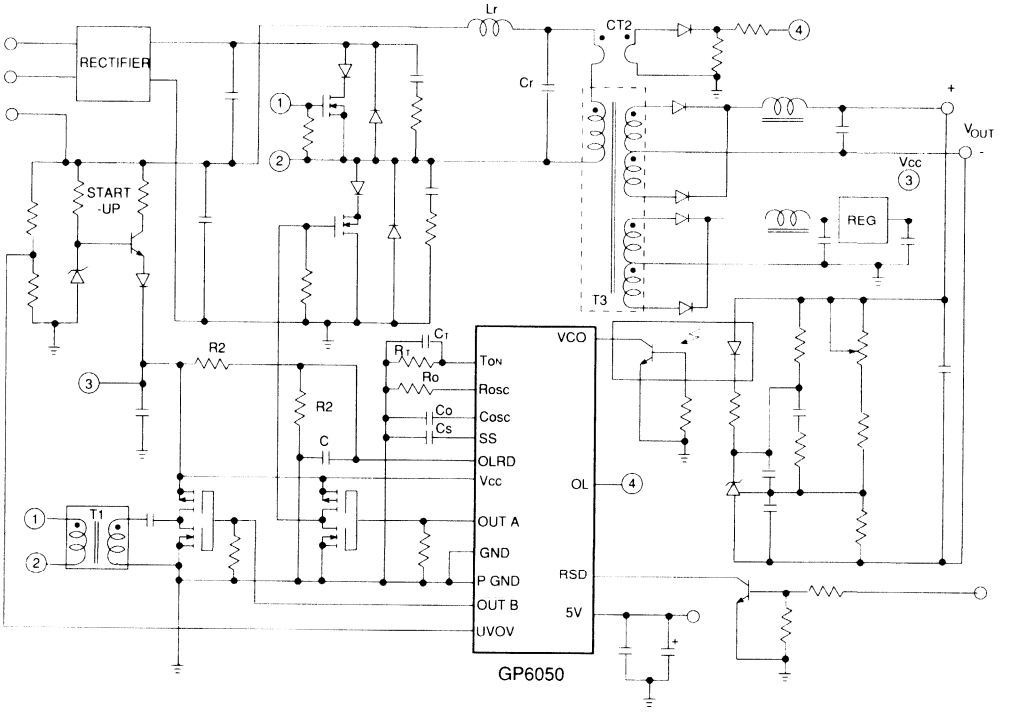


Fig. 12 Typical GP6050 Application

RMD 2

AVAILABLE PACKAGING

16 pin DIP and 16 pin SOIC

CAUTION

ELECTROSTATIC

SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC FREE WORKSTATION

GENNUM CORPORATION

Single-ended Resonant Mode Power Supply Controllers

GP6040 and GP6041
PRELIMINARY DATA SHEET

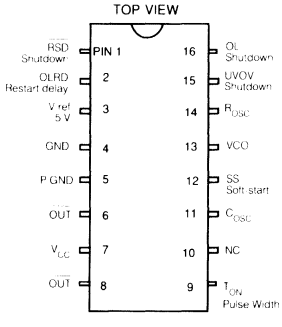
RMD 3

FEATURES

* frequency range of 1 kHz to 3 MHz
* operating frequency range set by a resistor (max.) and a capacitor (min.)
* pulse width set by a resistor and capacitor
* low start-up current
* synchronous overload shutdown with delayed soft restart
* synchronous overvoltage, undervoltage and remote shutdown
* soft-start
* single-ended output
* drives power MOSFETs directly (1.6A peak)
* low cost 16 pin DIP or SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	20V
Undervoltage/Overvoltage Input	-0.4V - 6V
Overload Input	-0.4V - 6V
Remote Shutdown	-0.4V - Vcc
VCO Input	-0.4V - Vcc
Storage Temperature	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec.)	260°C
Junction Temperature	150°C
Power dissipation at T_A ≤ 70°C (derate 9 mW/°C for T_A > 70°C)	720 mW



PIN CONNECTION
16 PIN DIP

CIRCUIT DESCRIPTION

The GP6040 and GP6041 are highly reliable, single-ended, resonant mode power supply controllers. These devices support resonant and quasi-resonant topologies operating in variable frequency mode. The pulse width is held constant while the frequency is varied by a feedback voltage over an operating range. Maximum and minimum frequency is set by an external resistor and capacitor. Fixed pulse width is adjusted by an external RC network.

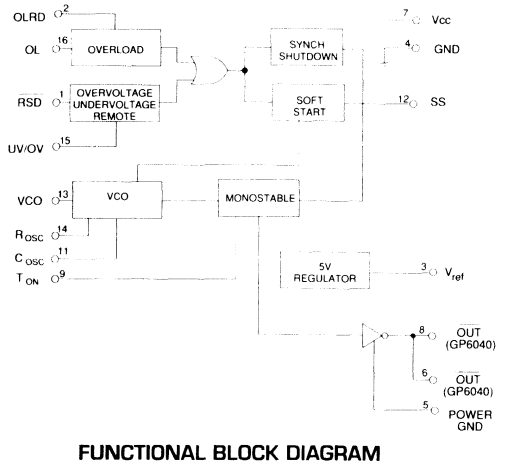
The single totem pole output has a 1.6 A peak current capability. The GP6040 provides active low driver output. The GP6041 provides active high driver output.

The high operating frequency of up to 3 MHz results in significant reductions in EMI noise and minimizes the size of the required magnetic and capacitive components in the power supply.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed.

The controller also contains power supply undervoltage lockout, minimizing supply current during the start-up condition.

The GP6040 and GP6041 are upgraded single-ended, pin-to-pin compatible versions of the GP605.



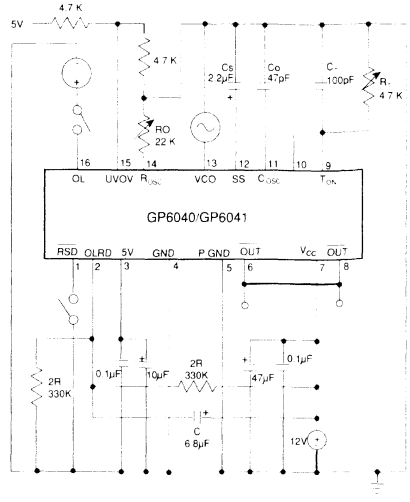
FUNCTIONAL BLOCK DIAGRAM

Document No. 510 - 59 - 1

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 2-6-2 Takanawa, Minato-ku, Tokyo 108

Part Number	Package Type	Temperature Range
GP6040 CD GP6041 CD	16 Pin DIP	0° to 70° C
GP6040 CK GP6041 CK	16 Pin SOIC	0° to70° C
GP6040 ID GP6041 ID	16 Pin DIP	-25° to 85° C
GP6040 IK GP6041 IK	16 Pin SOIC	-25° to 85° C
GP6040 M GP6041 M	TBD	-55° to 125° C

ORDERING INFORMATION



OPEN LOOP TEST CIRCUIT

ELECTRICAL CHARACTERISTICS

Limits apply over
0°C ≤ T_A ≤ 70°C for the GP6040/41CD, andGP6040/41CK
-25°C ≤ T_A ≤ 85°C for the GP6040/41ID and GP6040/41IK
-55°C ≤ T_A ≤ 125°C for the GP6040/41M

Parameters tested on open loop test circuit
Typical values are at T_A = 25°C
* Parameters marked with an asterisk* are valid only at T_A = 25°
V_{CC} = 12V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Chip Enable V_{CC} Threshold		11.3	12	12.7	V
V_{CC} Undervoltage Lockout		8.5	9.0	9.5	V
Supply Current	Undervoltage condition Normal condition	- 18	5 22	- 24	mA mA
Voltage Control Oscillator					
Maximum Frequency		2.4	3	-	MHz
Tolerance of *f*max Tolerance of *f* min	Fig. 6 Fig. 5	- -	- -	±5 ±20	% %
Temperature coefficient *f*max Temperature coefficient *f*min		-300 400	-600 700	-900 1000	ppm/°C ppp/°C
Dead Time T_{OFF}*		-	50	75	ns
Operating Range of VCO Input (Pin 13)	max min	- -	6.5 1.1	- -	V V
Linearity of the VCO		-	-	±5	%
Internal Pull-up Resistor (Pin 13)		8	10	12	kΩ
Output Pulse Width T_{ON} Tolerance		-	-	±5	%
Temperature Coefficient of T_{ON}		0	400	800	ppm/°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Risetime	100pF II 100 kΩ load on OUT	-	20	40	ns
Output Falltime		-	15	30	ns
Output Low Level (sink)	20mA	-	-	0 7	V
	200mA	-	-	2 2	V
Output High Level (source)	-20mA	-	-	Vcc -2	V
	-200mA	-	-	Vcc -2 2	V
Reference Section					
Output Voltage*		4 75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Max Current Capability		-	10	-	mA
Shutdown Section					
Soft-start (1)	C_S = 2 2 µF, VCO = 7V	16	19	22	ms
Overload Restart Delay	2R = 330 kΩ, C = 6 8 µF	1.0	1 3	1 6	s
Propagation Delay to Shutdown (3)		-	200	300	ns
Remote Shutdown (2)	Enabled	Vcc -0 8	-	-	V
	Disabled	-	-	3	V
Overload Shutdown (OL) Threshold*		2 84	3 0	3 16	V
OL Threshold Temp. Coefficient		-400	100	500	ppm/°C
OL Hysteresis		-	3	-	%
OL Trigger Pulse Width		500	-	-	ns
OL Input current Range		-1	-	+15	µA
Overvoltage Threshold* Lockout		2 84	3 0	3 16	V
Undervoltage Threshold* Lockout		-	1 9	2 0	V
Temp. Coeff. of Thresh'd Voltage		-400	100	500	ppm/°C
Hysteresis of the Lockout Voltage		-	3	-	%
Input Current Range (Pin 15)		-1	-	+22	µA
Thermal Impedance	16 pin DIL Plastic Package θ JC	-	42	-	°C/W
	16 pin DIL Plastic Package θ CA	-	70	-	°C/W
	16 Pin SOIC θ JA	_	112	-	°C/W

NOTES

(1) Soft-start time is measured from output enable at minimum frequency to time at which maximum frequency is reached.

(2) Refer to pin description for current required.

(3) If the shutdown input is triggered 200 ns before the next output pulse is expected, there will be no pulses. If there is a pulse earlier than 200 ns, this pulse is completed in full before the output is disabled. This is known as synchronous shutdown, a necessary feature in any resonant mode controller.

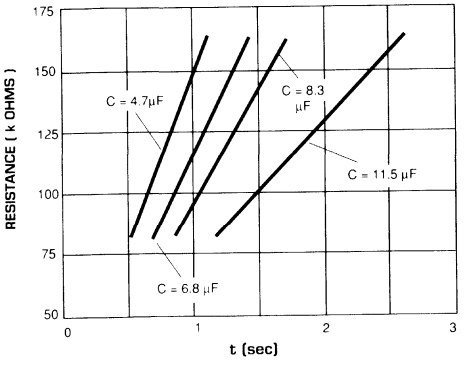


Fig. 1 Overload Restart Delay

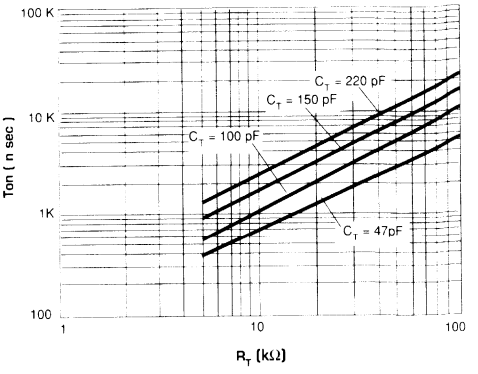


Fig. 2 Output Pulse Width

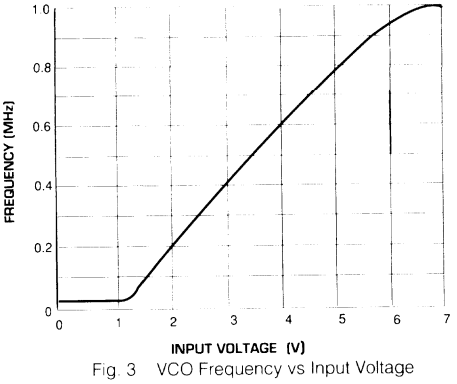


Fig. 3 VCO Frequency vs Input Voltage

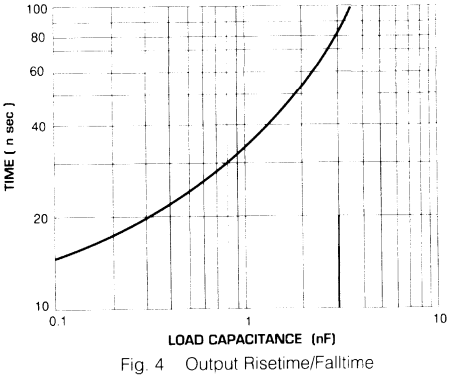


Fig. 4 Output Risetime/Falltime

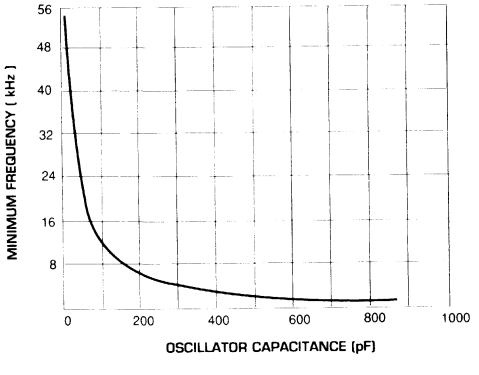


Fig. 5 Minimum Operating Frequency

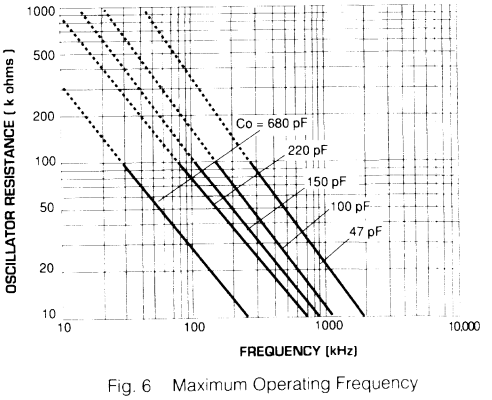


Fig. 6 Maximum Operating Frequency

TYPICAL PERFORMANCE CURVES OF THE GP6040 AND GP6041
For all graphs, *Vcc* = +12 volts DC and T_A = 25 °C. The curves shown above represent typical batch sampled results.

PIN FUNCTIONS

The GP6040 and GP6041 are complex devices, so the best place to start is with a functional pin description.

Pin 1 (*RSD*) - Remote Shutdown
A low on pin 1 shuts down the controller. When the pin is released the controller goes into soft-start. This pin is normally driven by an open collector transistor where the current is given by:

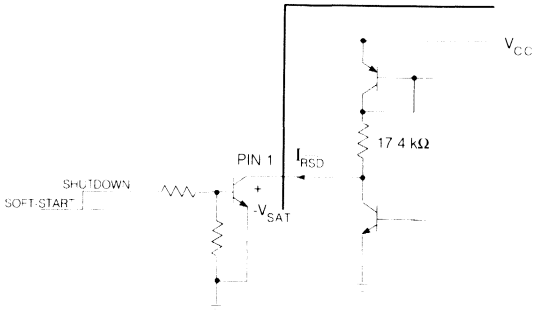


Fig. 7

$$I_{RSD} = \frac{(V_{CC} - V_{SAT} - 0.7)V}{17.4\ k\Omega} \quad mA \pm 20\%$$

For CMOS or bipolar circuitry, the configuration may be:

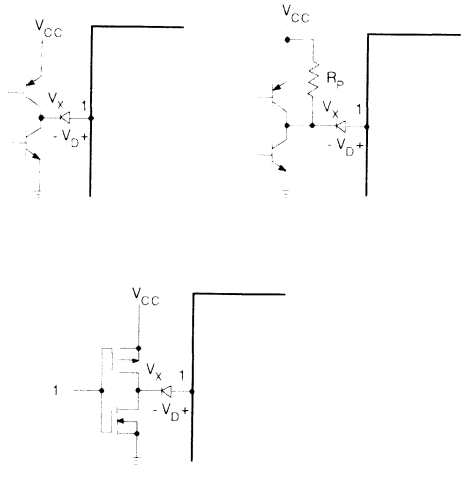


Fig. 8

In all cases the voltage must pull up to a minimum of

$$V_X = V_{CC} - 0.8V$$

assuming diode voltage $V_D \approx 0.4V$ when it is off (non-conducting). If remote shutdown is not used, leave pin 1 open.

Pin 2 (*OLRD*) - Overload Restart Delay
A 330 kΩ + 330 kΩ voltage divider in combination with a 6.8 µF capacitor generates a 1.3 second shutdown to restart delay every time the overload sense (pin 16) is activated. Timing starts when the overload is removed; upon timeout soft-start begins. Refer to Figure 1 to select RC combinations for other delays.

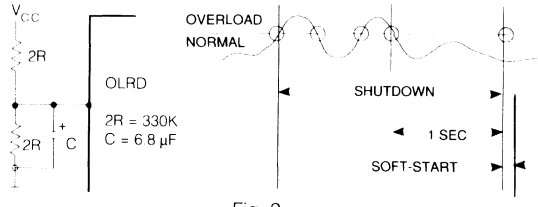


Fig. 9

RMD 3

Pin 3 (*5V*) - 5V Reference
This is a 5% tolerance regulator used to power most of the internal circuitry. To improve noise rejection it is recommended to decouple this pin with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor. Pin 3 can be used as a reference for any external circuitry as long as the load is less than 10 mA.

Pin 4 (*GND*) - Analog Ground
Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimized and do not interfere with feedback voltages and the reference.

Pin 5 (*P GND*) - Power Ground
Only the output transistors are connected to the power ground, to minimize interference with the logic circuitry. *GND* and *P GND* are to be connected outside the package, with the decoupling of the supply to this point.

Pin 6, 8 (*OUT*) - Output
Pins 6 and 8 are internally shorted together. The GP6040 provides an active low output driver during fixed pulse width. The GP6041 provides an active high output driver during fixed pulse width. For proper operation, the voltage on the output pins must not go below ground potential or above V_{CC} by more than 0.5 V.

Pin 7 (V_{CC}) - Supply Voltage
The power supply trace must be decoupled as close to pin 7 as possible. Currents of 0.5 A levels may be drawn by the GP6040 and GP6041. Minimum recommended decoupling is with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 9 (T_{ON}) - Pulse Width

The fixed pulse width T_{ON} is set by a resistor R_T and capacitor C_T. This relationship is shown in Figure 2. $R_T \times C_T$ should have a temperature coefficient of -500 ppm/°C for best stability and fall within the following ranges:

$$5\ k\Omega \leq R_T \leq \text{no limit}$$
$$47\ pF \leq C_T \leq 100\ nF$$

The R_T and C_T should be connected as close as possible to *GND* to minimize ground noise variations. The upper limit on pulse width is determined by chip-to-chip variation, power supply and component tolerances. The worst case combination must give $T_{ON} < 1/f\text{max} - T_{OFF}$, where T_{OFF} = 50 ns typ. (75 ns max.). The off period is required by the design of the controller. The pulse width T_{ON} should be set to give an off period greater than T_{OFF} so that the circuit will operate correctly at $f$max, where f is the actual operating frequency. Rewriting the equation as:

$$T_{OFF} = 1/f - T_{ON}$$

The GP6040 or GP6041 will divide the output frequency by two when T_{OFF} decreases to 50 ns. This is a failsafe feature to ensure the pulse width will never be incorrect by limiting $f$max. Under normal operation $f$max should be limited using R_{OSC}.

Pin 10 - Not Connected

Pin 11 (C_{OSC}) - Oscillator Capacitor

The capacitor C_{OSC} on this pin, controls the minimum frequency $f$min of the *VCO* operating range. Refer to Figure 5 for selection. Layout is critical for this component, keeping leads as short as possible and connecting close to the *GND* pin.

Pin 12 (*SS*) - Soft-Start

A capacitor C_S on this pin provides a controlled start up from $f$min to $f$max. The delay is approximately $t_{SS}(ms) \approx 8.7\ C_S(\mu F)$ for C_S between zero and 47µF.

To ensure a full soft-start duration when soft-start is caused by an undervoltage or overvoltage fault, it is necessary to have the fault present for about half the soft-start time.

Pin 13 (*VCO*) - Voltage Controlled Oscillator Input

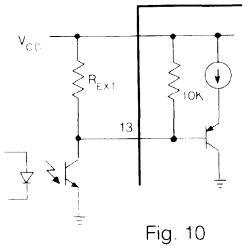


Fig. 10

The VCO input is designed for an optocoupler feedback network from the secondary (output) side of the power supply. An internal 10 kΩ pull-up resistor is provided but an external resistor may be used if a lower value is required. The control characteristic is shown in Figure 3. The linear input range is from 1.1 V to 6.5 V where 1.1 V represents $f$min and 6.5 V represents $f$max.

Pin 14 (R_{OSC}) - Oscillator Resistor

The resistor R_{OSC} on this pin, controls $f$max, the maximum frequency of the *VCO* operating range. C_{OSC} the capacitor controlling $f$min must be selected first, then refer to Figure 6 for selection of R_{OSC}. For good stability, a 1% resistor with a temperature coefficient of -600 ppm/°C, is recommended. Minimum value for R_{OSC} is 10 kΩ.

Pin 15 (*UVOV*) - Undervoltage/Overvoltage

The input is a window comparator. A higher or lower voltage than the thresholds specified will shut down the power supply until voltage falls within the window again, at which point the controller goes into soft-start. If pin 15 is not used, it must be tied to V_{CC} or the 5V reference via a voltage divider, generating a bias voltage, which falls within the window. The voltage divider should carry approximately 1 mA. The maximum input voltage on this pin is 6 V.

Pin 16 (*OL*) - Overload Input

A voltage exceeding the specified threshold on this pin will cause the controller to shut down and activate the overload restart delay function. This delay starts when the input voltage drops below the threshold. On time-out, soft-start begins. The maximum input voltage on this pin is 6V. If pin 16 is not used, short it to ground. No capacitor is required on pin 2 (*ORLD*), but a bias voltage between $V_{CC}/3$ and $V_{CC}/3$ + 5.7 V is still needed. A convenient voltage is $V_{CC}/2$.

A TYPICAL APPLICATION CONFIGURATION

Figure 7 shows the GP6040 as a resonant mode power supply providing 5V DC output. Capacitors *C4 and C32* in series with inductor L_r form the resonant tank. The load transformer *T1* is attached in parallel to resonant tank capacitors. For more information, request parallel resonant mode converter Application Note 510-63.

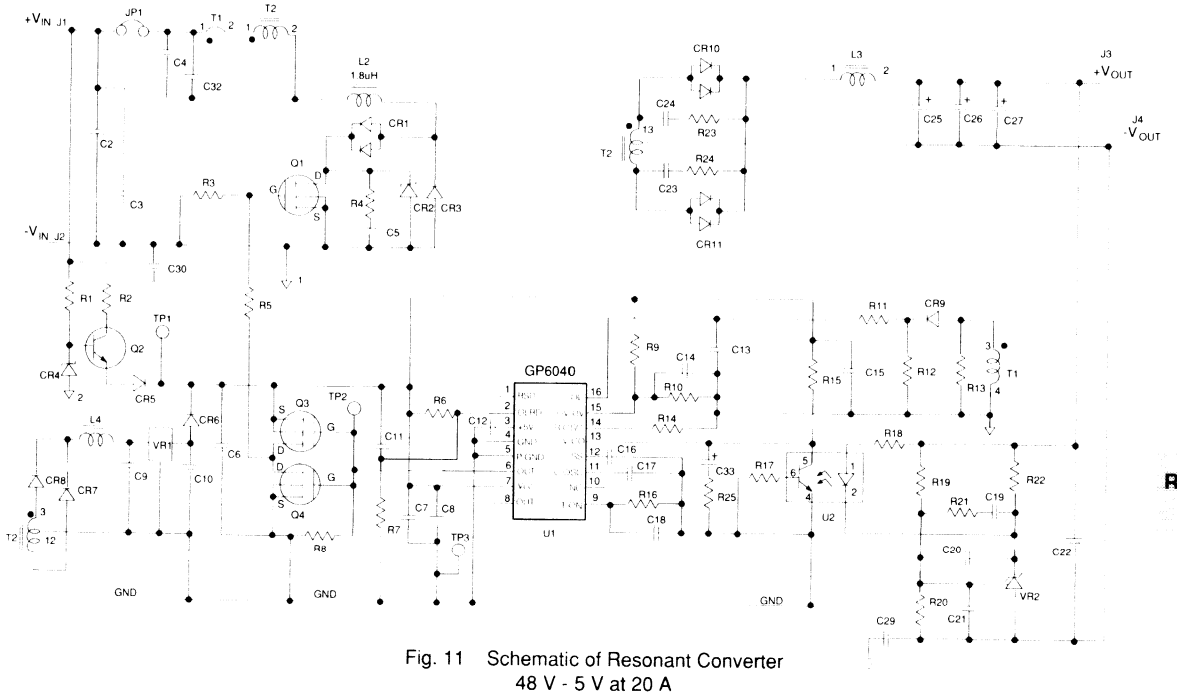


Fig. 11 Schematic of Resonant Converter
48 V - 5 V at 20 A

AVAILABLE PACKAGING
16 pin DIP and 16 pin SOIC

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

GENNUM CORPORATION

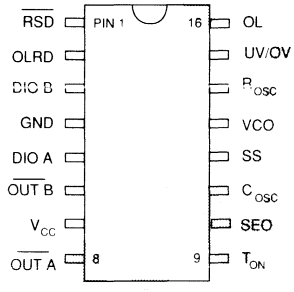
Monolithic 4x1 Video Crosspoint Switch

GX414A PRELIMINARY DATA SHEET

FEATURES

* **frequency range of 10 kHz to 1 MHz**
* **operating frequency range (min. and max.) set by a resistor and capacitor**
* **pulse width set by a resistor and a capacitor**
* **synchronous overload shutdown with restart delay**
* **synchronous overvoltage, undervoltage and remote shutdown**
* **soft-start**
* **single-ended or complementary outputs**
* **drives power MOSFETs directly**
* **low cost 16 pin DIP or SOIC**

TOP VIEW



PIN CONNECTION
16 PIN DIP

CIRCUIT DESCRIPTION

The LD405 utilizes frequency modulation instead of pulse width modulation to achieve regulation. The pulse width is held constant while the frequency is varied over an operating range set by a resistor and capacitor. A feedback voltage controls the switching frequency of the two complementary outputs, which are capable of driving power MOSFETs directly.

RMD 4

Opening a normally grounded control pin puts the LD405 into single-ended operation. In this mode the frequency is doubled and the two outputs are identical so they can be paralleled for increased drive capability. The high operating frequency of up to 1 MHz results in significant reductions in the size of the required magnetic and capacitive components. This leads to dramatic savings in volume, weight and manufacturing cost of switching power supplies.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
LD405D	16 Pin DIP	0° to 70° C
LD405K	16 Pin SOIC	0° to 70° C

CAUTION
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The GP605 in a Variable Frequency Zero Current Switching, Half Bridge Resonant Mode Power Supply

APPLICATION NOTE

1.0 INTRODUCTION

The continuous trend towards reducing the size of power converters forces designers to increase operating frequencies. Conventional quasi-square pulse converters are now approaching the 300 to 500 kHz range. This allows about a 3:1 reduction in the size of the major passive components, such as magnetics and capacitors, as compared to 20 kHz switchers. But these converters (mostly pulse width controlled converters), obviously have higher switching losses in power semiconductors (see Figure 1a), despite the use of MOSFETs. The resulting inefficiency requires larger heatsinks, and thus defeats the goal of reducing the size.

There is, however, a more efficient way to convert power at ever higher frequencies. It is called *zero current switching* or *sinewave current switching* (see Figure 1b). Such a waveform can be generated by either a parallel or series resonating LC tank. The resulting class of converters is called *resonant*.

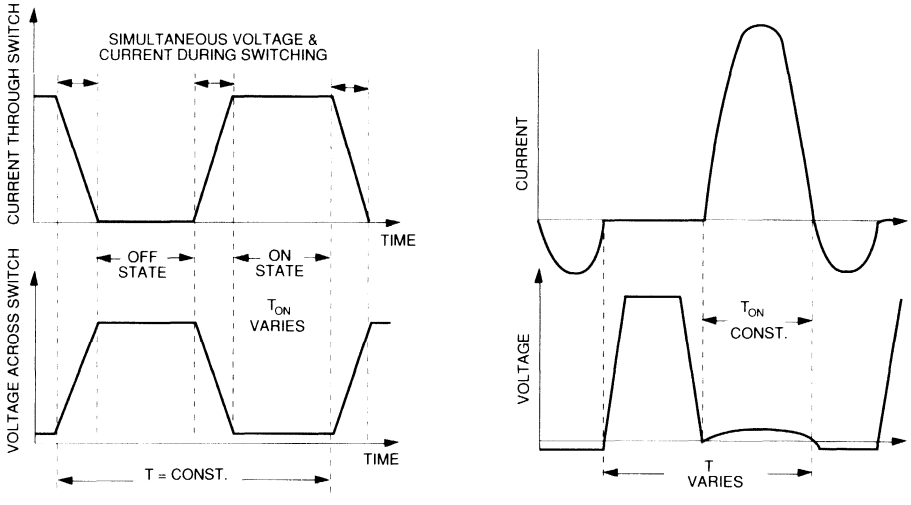
The clear advantage of sinewave current is that, as switching generally occurs at zero current, switching losses in power semiconductors are almost eliminated. The primary disadvantage of a resonant converter is that for a given power level, the actual peak current is 3 to 4 times greater than that of a PWM converter. This can be overcome by using lower *on resistance* semiconductors, creating a practical means to increase operating frequencies up to 1 MHz and higher. These frequencies allow designers to achieve power densities in excess of 25 watts/cubic inch, which is about 4 times better than is possible at 100 kHz.

There are many types of resonant and quasi-resonant topologies. Besides a sinewave switching current, most of them employ FM control, which provides a fixed *on time* (T_{ON}), and variable period *T*. Conversely, PWM uses fixed period, variable *on time*.

This application note describes a 125W resonant mode power supply, with Gennum's GP605 performing both control and housekeeping functions.

The GP605 is an upgraded version of the first commercially available resonant mode controller - Gennum's LD405. This IC combines all the necessary features of modern power controllers.

If you are not familiar with the GP605 please refer to Gennum's data sheet 510-43.



1a) PWM 1b) FM

Fig. 1 GP605 Block Diagram

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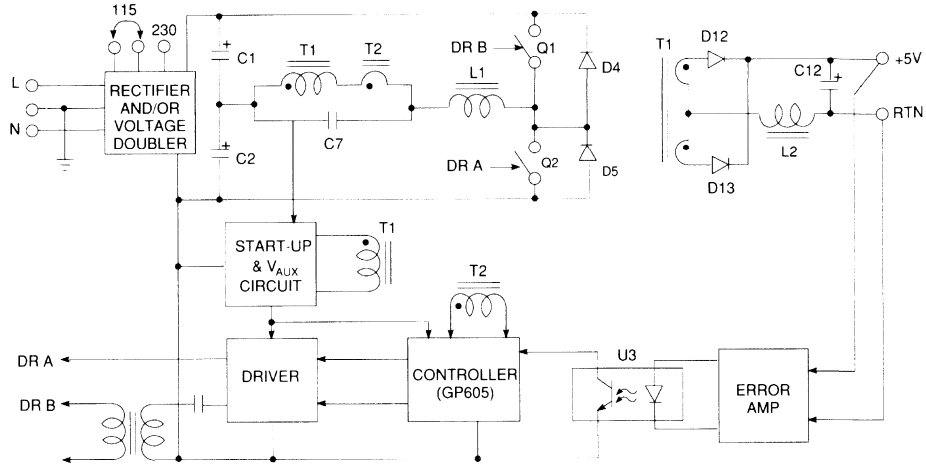

Fig. 2 Block Diagram of an Off-line Unit (115V AC or 230V AC)

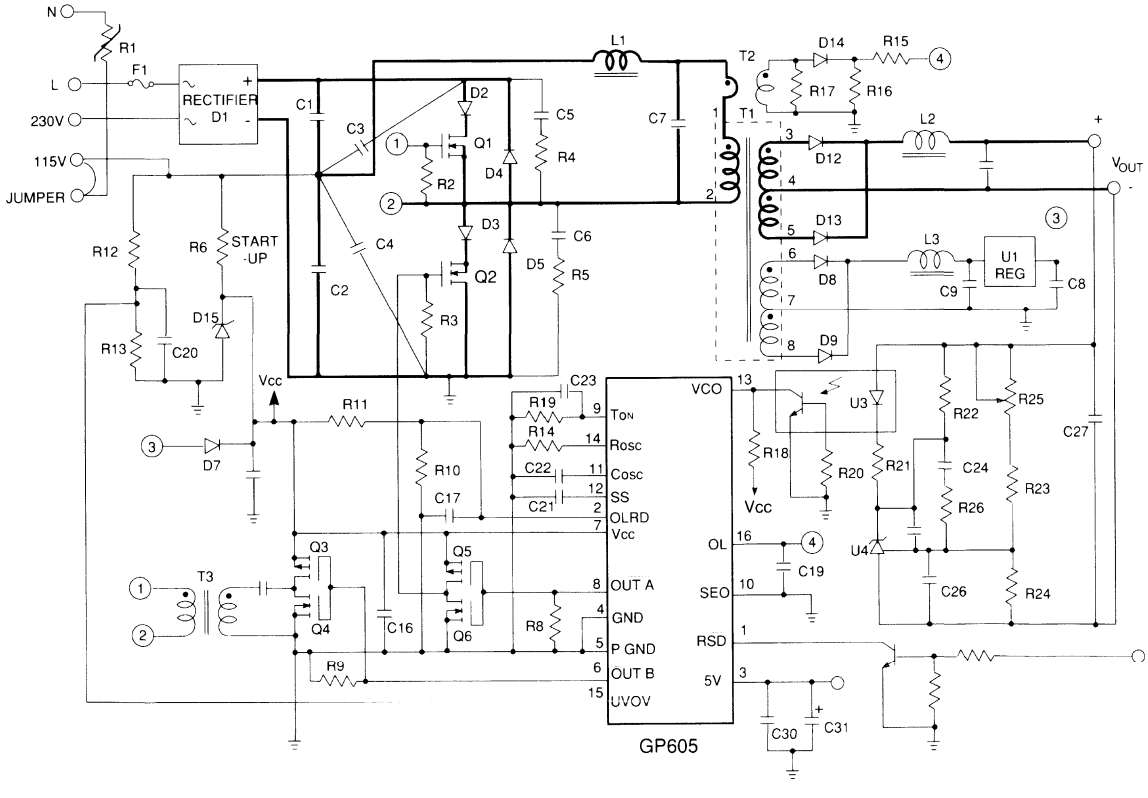

Fig. 3 Detailed Schematic of the Supply for Figure. 2

2.0 RESONANT POWER SUPPLY

A Rectifier/Voltage Doubler block provides an unregulated 300V DC (*VNR*) bus for the high frequency resonant converter. A resonating tank, consisting of an inductor *L1* and capacitor *C7*, is connected in series. Sinusoidal voltage across the capacitor *C7* to the output stage is stepped down via the power transformer *T1*. As far as the driving sequence is concerned, this resonant converter operates similarly to a half bridge square pulse converter. During the first resonating cycle switch *Q2* is off. The full cycle takes place in *Q1*, the parallel combination of *C7* and the primary winding on *T1* (along with one turn of the current sense transformer *T2*), and inductor *L1*. The return current flows via diode *D4*. Capacitor *C1* serves as a voltage source for this cycle.

In the second resonating cycle switch *Q2* is on and *Q1* is off. The second cycle takes place in *Q2*, the inductor *L1*, and the parallel combination of *C7*, and the primary winding on *T1* (again one turn on the current sense transformer *T2*). The return current in this case flows via diode *D5*. Note that the current in the second cycle has reversed its polarity as compared to the current in the first cycle, thus transformer *T1* works in a bipolar mode. Capacitor *C2* serves as a voltage source for the second cycle. During the period of time when switch *Q2* is off, diode *D4* clamps the voltage across *Q2* to the level of the *VNR* bus. The diode *D5* does the same thing for switch *Q1*. Thus switches *Q1* and *Q2*, as well as diodes *D4* and *D5*, can be rated to only 420 volts. Therefore the high line (132V AC RMS or 264V AC RMS) after being doubled and rectified, still leaves a safety margin of about 50 volts.

The output stage is fairly straightforward. It is a full-wave Schottky, centre-tap rectifier, composed of *D12*, *D13*, *L2*, and output capacitor *C12*. The output here is 5V DC at 25 amps.

Regulation is achieved by changing the commutating frequency of the controller GP605. Its VCO gets the input signal from an error amplifier via the optical coupler *U3*. The controller also performs the following functions:

- soft-start
- hiccup current limit
- VNR bus undervoltage and overvoltage shutdown
- remote shutdown

In order to provide fast turn-on and turn-off of the power switches *Q1* and *Q2*, driving requires an additional stage. Although the average power needed to drive both switches is under 1 watt, it takes up to 0.75A of short-duration current pulses to charge and discharge the gate source capacitance of the MOSFET switches *Q1* and *Q2*. This is achieved by using *totem-pole* type MOSFET stages. Transistors *Q5* and *Q6* drive switch *Q2*, while transistors *Q3* and *Q4* drive switch *Q1* via a pulse transformer *T3*.

The controller and driver are powered by the 12V DC V_{AUX} bus. During start-up this voltage is supplied from one half of the VNR bus via thermistor *R6*, and zener diode *D15*.

About 18V is supplied to the V_{AUX} bus on start-up. Once the supply is up and running (about 20 ms) V_{AUX} is supplied by the additional winding, 6-8, of the power transformer *T1*. The voltage from this winding is rectified and regulated to the level of 12V ±5%.

The supply utilizes primary current sensing. This involves the primary winding of the power transformer *T1* being connected in series with a single turn winding of the $^1/_4$ inch diameter current-sensing transformer *T2*. This transformer has a turns ratio of 1:40. Its secondary winding voltage is in linear proportion to the primary winding current, and the voltage pulses look like current pulses in the primary of the power transformer *T1*.

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After rectification and some filtering, an essentially *sawtooth* voltage level, (which is proportional to the total load), is applied to pin 16 of the controller. Once this *sawtooth* reaches a programmed threshold, the controller shuts down for approximately 1 second. This waiting period is set by a 4.7 µF tantalum capacitor connected to pin 2. When it has elapsed, the controller starts generating its *pulse-train*. Initially the pulse frequency is approximately 10 kHz, then increases, following a preset time constant. In about 20 ms the power supply either reaches a normal regulation mode, or if the overload condition on the output continues, it goes into shutdown again. The supply will stay in the *hiccup* mode until the overload is removed.

The maximum commutating frequency of this supply is 600 kHz (300 kHz per transistor) and the resonating frequency of the *C7-L1* tank is about 750 kHz.

The value of *C7* is 8200 pF and the value of *L1* is 5 µH. The resonating frequency f_r can be calculated from the following equation:

$$f_r = \frac{1}{2\pi \sqrt{C_r L_r}}$$

where C_r and L_r are resonating components.

The primary power transformer winding inductance is at least 100 times higher than that of *L1*, therefore it does not affect the resonating frequency f_r.

3.0 DESIGN SEQUENCE

3.1 Integrating the GP605 into the Power Supply

3.1.1 Maximum VCO Frequency

In this design f_{max} is set at 600 kHz. For the oscillator capacitor (C_{OSC}), a temperature stable NPO (COG), ceramic, 150 pF capacitor is recommended. Keep the leads on this capacitor very short to minimize the parasitic inductance. According to Gennum's data sheet 510-43, R_{OSC} - 17.4 kΩ, 1%. Tolerance of *fmax* from chip to chip is ±5% (570 kHz to 630 kHz).

3.1.2 Set Output Pulse Width (T_{ON})

The timing for the MOSFET switch *Q1* (*Q2*) is set to shut off during the diode *D4* (*D5*) conduction, (see Figure 1). The best method of doing this is to terminate the T_{ON} pulse right in the middle of a negative half of a sine wave current:

$$T_{ON} = 0.75 \frac{1}{f_r}$$

Then relative inaccuracy in T_{ON} will not affect the circuit 's operation. In this case f_r =750 kHz, and T_{ON} = 1 µs. A 100 pF capacitor is chosen and placed in series with R_T (*R19*) whose value is determined to be 9.4 kΩ, as seen from the graph (Figure 2) in data sheet 510-43.

3.1.3 Soft-start Capacitor

Capacitor *C21* is needed to provide a relatively slow change in the *VCO* operating frequency , from minimum value (about 11 kHz for C_{OSC} = 150 pF) to the value which is set by the feedback loop. The result is a soft start-up of the power supply. Usually 2 to 3 cycles of the input AC line are sufficient to charge the input filter capacitors. This means that 30 ms to 48 ms Soft-start Delay (50-60 Hz) is necessary. A 4.7 µF capacitor value provides about 40 ms of soft-start (see 510-43 data sheet pin description). The higher the power level of the converter, the longer the soft-start time is needed. A value of 100 to 200 ms could be used for a 500 W supply.

3.1.4 VCO Input

In this application design, the input voltage is set by an error amplifier via an optocoupler.

The proper level of the current in the photo-transistor is set by an external resistor *R18*. If the VCO input is set at 4.0V, (in the middle of the 1.5V - 6.5V range of VCO), and V_{CC} = 12V, the parallel combination of 10 kΩ internal pull-up resistor and external *R18* resistor, is about 2.3 kΩ. Thus *R18* = 3 kΩ.

3.1.5 UVOV Shutdown

This pin is used to set the input voltage operating range for the power supply. The nominal value for the rectified 220V AC bus is about 350V (taking input diode drops into consideration). Normally this pin level is set to 2.5 volts.

Resistive divider *R12* - *R13* carries just under 1 mA of current. Having *R12* = 360 kΩ and *R 13* = 3 kΩ sets up the range from 220V DC (78V AC x 2 x 1.4) to 390V DC (138 V AC x 2 x 1.4) which is quite acceptable for most designs. To change undervoltage and overvoltage threshold levels, apply resistance between UVOV input (pin 15) and reference voltage (pin 3)(Fig. 4).

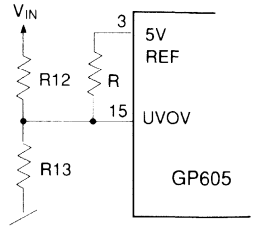

Figure 4

The value of the resistors can be calculated from the equations:

$$R = \frac{(V_o \times V_r) - (V_u \times V_r)}{(V_u \times V_{ino}) - (V_o \times V_{inu})} \times R12$$

$$R13 = \frac{R12 \times V_r \times (V_o - V_r)}{V_r \times (V_{ino} - V_{inu} + V_u - V_o) + (V_o \times V_{ino} - V_u \times V_{ino})}$$

where
- V_o - the GP605 overvoltage threshold lockout
- V_u - the GP605 undervoltage threshold lockout
- V_r - reference voltage
- V_{ino} - requested line overvoltage lockout
- V_{inu} - requested line undervoltage lockout

3.1.6 Overload Protection (OL)

The current sensing is provided by the current transformer *T2*. With a turns ratio of 1 : 40 it reduces the primary current of the power transformer *T1*, by a factor of 40. Only positive pulses pass by diode *D14*. The resulting voltage drop across resistor *R16*, is applied to pin 16 (OL) of the GP605 via resistor capacitor filter *R15* - *C19*. The time constant of this filter is 3.5 µs. Therefore the voltage across *C19* looks like a saw tooth. Once the level reaches 3.2V (±0.3V), the controller shuts down the power converter for a period of time set by the capacitor *C17*. As *R11* = *R10* = 300 kΩ and *C17* = 4.7 µF, this overload restart delay is about 0.7 seconds. If the overload condition remains (look for a possible short on the output), the power converter will continue to try to come back on-line with 40 ms soft-start every 0.7 seconds. The resulting average current into the short will be very low, less than 0.05 I_{max}, where I_{max} is set by the value of *R16* and turns ratio of *T2*.

3.1.7 Driving Large Area MOSFETs

Although the output stages of the GP605 are capable of delivering 0.6A peak current, it might be beneficial to use buffer driving stages between the chip and large area MOSFETs. In order to charge 200 pF of gate-source capacitance in 100 ns, the driver stage must deliver up to 0.75 A_{peak} of short current pulses.

It can be achieved by a totem-pole, small signal MOSFET stage, *Q3-Q4* (*Q5 -Q6*). In this case the GP605 output drives only about 70 pF load. Both driver MOSFETs have $R_{DS_{ON}}$ of 8 Ω and can provide high current pulses to charge and discharge C_{gs} of power MOSFETs.

3.2 Power Transformer Design

The practical design starts with finding the turns ratio *'n'* between the primary winding (1-2) and the secondary windings (3-4) = (4-5) of the power transformer *T1*.

Assuming low line condition (V = 115V DC for a typical supply), the converter will operate with minimum dead-time (about 25%) and the voltage across the primary will be very close to an ideal sinewave $V_{1\text{-}2} = V \sin \omega_O t$,

$$n = \frac{0.707V}{1.25\,(V_{OUT} + V_F)}$$

Where V_{OUT} is the rectified output voltage and V_F is a forward drop across a Schottky diode.

For V_{OUT} = 5V, V_F = 0.5V, and V = 115V : n ≈ 12

In transformers above 500 kHz, the practical amount of turns for the 5V secondary winding is one turn.
Then (3 - 4) = (4 - 5) = 1 turn and (1 - 2) = 12 turns.
The fundamental relationship in the transformer is:

1. $$e = NA_e \frac{dB}{dt} \quad 10^{-8}$$

Where e is instantaneous voltage across a winding in volts, *N* is the number of turns in that winding, A_e is the transformer core area in cm^2 and *dB/dt* is the instantaneous rate of change of flux density in gauss per second.

2. $$\Delta B \text{ (over a Time } = \frac{T}{2}) = \frac{10^8}{NA_e} \int_0^{T/2} edt$$

where *T* is the operating period in seconds.

In the sinewave converter:

3. $$e = E \sin \frac{2\pi}{T} t$$

where *E* = sinewave peak.

4. $$\int_0^{T/2} edt = E \int_0^{T/2} \sin \frac{2\pi}{T} tdt$$

$$= E \left(-\frac{T}{2\pi} \cos \frac{2\pi}{T} \bullet \frac{T}{2} + \frac{T}{2\pi} \cos 0 \right) = \frac{ET}{2\pi}$$

5. $$\text{So } \Delta B = \frac{10^8}{NA_e} \times \frac{ET}{2\pi}$$

From this equation maximum operating flux density can be calculated:

$$B = \frac{10^8 \ V \bullet Tr}{2\pi \ N \bullet A_e}$$

B is in gauss, *V* is the peak voltage in volts, T_r is the period of resonating frequency in seconds, *N* = primary turns, and A_e = core area in cm^2.

For Magnetics core F - 43622 - UG,
A_e = 1.59 cm^2 nominal *V* = 150V. If resonating frequency of 750 kHz is chosen, then

$$B = \frac{10^8 \times 150V \times 1.33 \text{ sec} \times 10^{-6}}{2\pi \times 12 \times 1.59} = 166 \text{ gauss}$$

According to Magnetics Inc. Data, this will result in about 100mW/cm^3 core loss (F material). The 43622 core has a volume of 8.46 cm^3. Total core losses will be approximately 850 mW, quite acceptable for a 125 W transformer.

Winding Losses:
Skin depth can be calculated from this equation:

$$\delta = \frac{0.066}{f}$$

where δ is in meters, *f* is in Hertz.
For 750 kHz operation δ = 0.076 mm = 3 mils.
In a flat conductor both sides can be considered a surface. So, at 750 kHz frequency, 5 mils of copper foil can be considered a good choice for 1 turn, 25 amperes secondary winding. The average length of turn for this transformer is ALT = 0.244 ft.
Foil width is about 0.5 in.
Foil area is 0.5 in. x 0.005 in. = 0.0025 sq. in.
It is about the same as the area of #16 AWG wire, and it has a resistance of about 4 mΩ per foot. So the resistance of 1 turn of foil is about 1 mΩ. In a full wave secondary winding of this power transformer, one can assume that I_{RMS} (secondary) = 25A and *R* = 1 mΩ then power dissipation in the foil:
P (secondary) = I_{RMS}^2 (sec) x *R* sec = 625 mW.
Conservative estimate for I_{RMS} (primary)

$$I_{RMS} \text{ (primary)} = \frac{I_{RMS} \text{ (sec)}}{12\,\eta}$$

where η is the efficiency of the supply (0.75 is the design goal).

Then I_{RMS} (primary) = $\frac{25A}{12(0.75)}$ = 2.78A

The #30 AWG wire would be a good choice for the primary winding; because it has a diameter of only 10mils this wire is quite efficient at 750 kHz.

Due to skin effects however, its DC resistance value has to be multiplied by 1.5 to obtain the true AC resistance at 750 kHz. The DC resistance of #30 wire is 100 mΩ per one foot. So the AC resistance will be 150 mΩ per one foot. Twelve primary turns have the total length of about three feet, therefore total AC resistance value of one strand is 0.45 Ω. Six strands in parallel will have resistance of R_{pri} = 75 mΩ. Then power dissipation in the primary:

$$P_{pri} = I^2_{RMS\ pri} \times R_{pri} = (2.78)^2 \times 0.075 = 580\ mW$$

Total Transformer Power Dissipation

$$P_T = P_{core} + P_{sec} + P_{pri} = 850\ mW + 625\ mW + 580\ mW = 2055\ mW$$

Rule of thumb is that in a well designed switching power supply, total losses in the transformer should not exceed 2% of the output power. In this case 2W transformer losses represent about 1.6% of the output.

The primary winding in this design is split into two halves, each half is 6 turns of 6 strands of #30 wire. The secondary windings are sandwiched between these halves. Such construction greatly reduces the leakage inductance and enhances power conversion.

3.3 Resonating Tank

It is always a challenge to choose the right value for C_r and L_r. If the inductor is too small, the excessive peak currents will make the design inefficient. If the inductance L_r is too high, the amount of power available for conversion will be limited. A good starting point is:

$$P_{OUT} = \frac{C_r V^2_{Cpeak}}{2} \bullet f$$

$$\text{Then } C_r = \frac{2P_{OUT}}{V^2_{C\ peak} \bullet f}$$

$f = f_{max}$ = 600 kHz at low line when $V_{c\ peak}$ = 220V

$$\text{Then } C_r = \frac{2 \times 125W}{(220V)^2 \times 600 \times 10^3} = 8608\ pF$$

The closest standard value is 8200 pF. Then L_r can be calculated from the equation

$$L_r = \frac{1}{C_r 4\pi^2 f_r^2}$$

for f_r = 750 kHz L_r = 5.5 µH

3.4 Power Semiconductor Selection

Every bidirectional switch in this supply actually consists of three power semiconductors, a Schottky diode *D2* (or *D3*), a MOSFET *Q1* (or *Q2*), and a fast recovery diode *D4* (or *D5*). The only purpose for *D2* is to block an internal parasitic diode of the power MOSFET. This internal diode is too slow for the purpose. Since the switches *Q1* and *Q2* operate out of phase, the maximum duty cycle for an individual MOSFET is about 38%. That happens at low line and maximum load, when $f = f_{max}$ = 600 kHz.

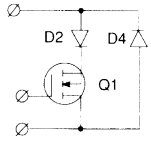

Figure 5

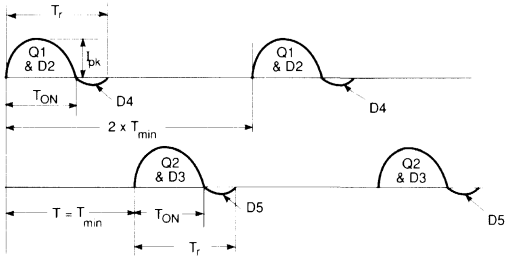

Figure 6

Under these conditions the return current via the diodes *D4* and *D5* almost disappears and peak currents in transistors reach 8A. So, I_{RMS} for *Q1* and *D2* will be the same as for *Q2* and *D3*:

$$I_{RMS\ (MOSFET)} = I_{peak} \sqrt{\frac{T_{ON}}{4T_{min}}}$$

$$\text{Since } T_{ON} = 0.38\ T_{min},\ I_{RMS} = 8A \sqrt{\frac{0.38}{4}} = 2.46A$$

The power dissipation in every transistor will be limited to conduction losses:

$P_{Q1} = P_{Q2} = (I_{RMS})^2 \times R_{dson}\ (T_j = 100°C)$

For IRFP450 MOSFET; $R_{dson}\ (T_j = 100°C)$

$= 1.7 R_{dson}\ (T_j = 25°C) = 1.77 \times 0.4\ \Omega = 0.68\ \Omega$

Then $P_{Q1} = P_{Q2} = (2.46A)^2 \times 0.68\ \Omega = 4.13\ W$

The efficiency can be improved by lowering the MOSFET junction temperature. For example, at 60°C IRFP450 maximum R_{dson} will be 0.52 Ω and losses will drop to 3.15W per transistor.

However, if IRF841 transistor is used, its

R_{dson} (T_j = 60°C) = 1.25 R_{dson} (T_j = 25°C) 1.25 x 0.85 = 1.06Ω

Then $P_{Q1} = P_{Q2}$ = 6.4 watts.

Although it is more efficient to use larger area MOSFETs, economical considerations may dictate the usage of IRF841 but at a lower junction temperature, (less than 60°C).

Schottky diode losses can be calculated from the following equation.

$$P_{D2} = P_{D3} = I_{RMS} \times V_{RMS}$$

where $V_{RMS} = V_{pk} \sqrt{\frac{T_{ON}}{2\,T_{min}}} = V_{pk} \sqrt{\frac{0.38\,T_{min}}{2\,T_{min}}} = 0.436\,V_{pk}$

Assuming $V_{peak} \approx 0.6V$ for a typical Schottky diode, $V_{RMS} \approx 0.26V$, and $P_{D2} = P_{D3} = 0.6$ watts. Return diodes *D4* and *D5* conduct very little current at nominal load. Only at light loads do they conduct significant current, and then, the duty cycle is very low. Although these diodes must be rated for up to I_{Q1peak} currents, they dissipate little power, approximately 0.5W each. Diodes must have 35ns - 50ns recovery time, so, $P_{D4} = P_{D5} = 0.5$ watts. Each power switch loss = $P_{Q1} + P_{D2} + P_{D4}$ = 6.4W + 0.5W = 7.5 watts. Both switches (six semiconductors) dissipate 15 watts.

OUTPUT SCHOTTKY

$P_{D12} + P_{D13}$ = 25A x 0.55V = 14 watts. Switching losses are low due to the sinusoidal character of the current.

3.5 Snubbers

These RC networks across power switches are needed to dampen voltage spikes. They reduce EMI and improve reliability.

Power losses:

$$P_{R4} = P_{R5} = \frac{C_5 V^2_{C5}}{2} \times \frac{f_{max}}{2} = \frac{47 \times 10^{-12}(220)^2}{2} \times \frac{6 \times 10^5}{2}$$

= 0.340W (low line, nominal load), total losses are 0.7W

It should be noted that at nominal line, snubber losses will be higher because they are proportional to V_C^2. For example, at nominal line

V_C = 300V and f = 350 kHz, then $P_{R4} = P_{R5}$ = 0.74 watts. Total losses will be 1.5 watts.

3.6 Power Supply Efficiency

Power switch losses	15.0W
Output Schottky diode losses	14.0W
Losses in snubbers	1.5W
Power Transformer losses (est)	2.0W
Control/drive circuits	1.0W
Output inductor dissipation (est)	2.0W
Resonating inductor dissipation (est)	0.5W
Input rectifier dissipation (est)	3.0W
TOTAL LOSSES	39.0W

Estimated efficiency $n = \frac{125W}{164W} \times 100\% = 76.2\%$

Measured efficiency $n = \frac{125W}{167W} = 74.8\%$

Additional losses totalling 3W are miscellaneous losses in device leads, printed circuit board etches, and proximity effect losses in the power transformer etc. A target for an off-line 5V output switching power supply is 75% efficiency.

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3.7 Possible Modifications to the Power Supply

This topology can be easily modified to achieve multiple output units. Additional windings can be placed on the power transformer as long as the total power does not exceed the rated value. Higher power supplies would require modification in the switches, transformers, as well as in the resonating tank. Output stages also would have to be *beefed-up*. The control circuit would require very minor modifications in the areas of current sensing and the compensation network.

4.0 PERFORMANCE ANALYSIS

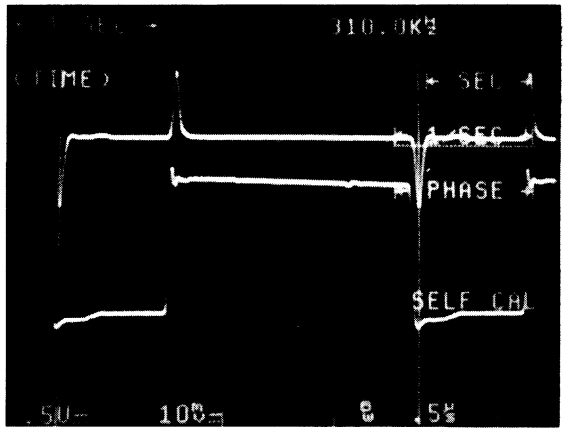
Among the most important characteristics of a power supply, are: efficiency, line and load regulation, transient response, and output ripple. The measured efficiency of the GP605 supply was approximately 75%. Line regulation (95V AC to 132V AC) was better than ±0.5 percent. Load regulation (5% to 100%) was better than ±1.5 percent. Total regulation band was better than ±2 percent. Transient response for 50% - 100% load-step was an excursion of less than ±5% of the output voltage, with total recovery under 500µs. Output ripple was less than 100 mV p-p.

All the above characteristics are quite acceptable for an off-line switching power supply.

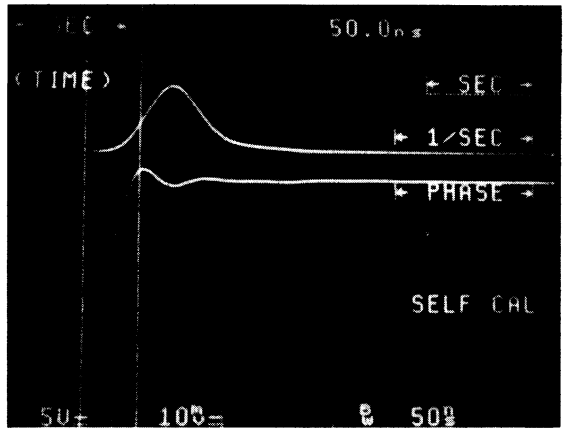
5.0 WAVEFORMS

Figure 7 shows the GP605 output driving totem-pole signal MOSFETs. Figure 8 shows the actual power supply resonating current versus GP605 outputs.

Fig. 7 Output Stage Driving Totem-pole MOSFETs
V_{CC} = 12V DC

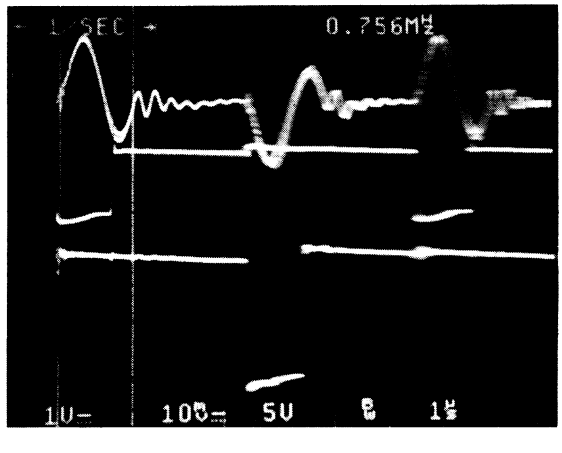


a) 0.5μs/div
Output Current 100mA/div
Output Voltage 5V/div



b) 50 ns/div

Fig. 8 Oscillograms of GP605 Output Stage Voltage and Power Transformer Current



Upper trace:
Power Transformer Primary Current
5A/div
1μs/div
Middle trace
Drive A Voltage 10V/div
Lower Trace
Drive B Voltage 5V/div

6.0 CONCLUSION

THhe GP605 provides an easy and cost effective way to control and protect resonant and quasi-resonant converters. The lack of suitable FM controllers has stopped many designers in the past from going to new topologies and higher frequencies. - now they have a choice.

References:

(1) Neville Mapham, "An SCR Inverter with Good Regulation and Sine-Wave Output," IEEE Trans. on Industry and General Applications, Vol.IGA-3, pp. I76-I87, March/ April 1967.

(2) Alex Estrov, "Power Transformer Design for 1MHz Resonant Converter" Proc. First High Frequency Power Conversion Conference" April I987, Intertec Communications, Ventura,California.

(3) N.O. Sokal and A.D. Sokal, "Class E - a new class of high-efficiency tuned single-ended switching power amplifiers," IEEE J.Solid-State Circuits, vol. SC-10, no. 3, pp. I68 I76, June 1975.

(4) Alex Estrov, Iain Scott, "FM Controller IC Supports up to 1 MHz Resonant supplies" PCIM, September 1987,Intertec Communications, Ventura, California.

RESONANT POWER SUPPLY BILL OF MATERIALS

C1, C2	Capacitoral.el. 330 µF 200V
C3, C4	Capacitor met.polypropolene 1µF 200V
C5, C6	Capacitor cer.NPO 47pF 1kV
C7	Capacitor cer.NPO 8200 pF 1kV
C8, C10, C11, C18, C30	Capacitor cer. X7R 0.22 µF 25V
C9, C31	Capacitor tant.conformally coated 4.7µF 35V
C16, C17, C21, C27	Capacitor tant.conformally coated 4.7uF I6V
C12, C13, C14, C15	Capacitor tant.conformally coated 220 µF 10V
C19, C24	Capacitor cer. X7R 0.022 µF 25V
C20, C26	Capacitor cer. NPO 1000 pF 25V
C22	Capacitor cer. NPO 150 pF ±5% 25V
C23	Capacitor cer. NPO 100 pF ±5% 25V
C25	Capacitor cer. X7R .047 µF 25V
C28, C29	Capacitor film 1000pF 250VAC 'Y' type
D1	Diode bridge 4A 600V Gen. Instr. KBU4J
D2, D3	Diode Schottky IN5823
D4,D5	Diode UFRD Amperex BYV29-500
D7	Diode IN4001
D8,D9	Diode UFRD Motorola MUR105
D10, D11, D14	Diode IN4148
D12, D13	Diode Schottky Motorola MBR3045PT (each)
D15	DiodeZener IN967A
F1	Fuse 5A 250VAC slo.blo.
L1	Inductor 5 µH ±5%, Core:Micrometals T51-8/90 12 turns of #28 AWG
L2	Inductor 7.5 µH ± 10%. Core: Arnold Eng. A-445146-2 or Magnetics 55344-A2. 7 turns of 5 strands in parallel #20 AWG.
L3	Inductor 330 µH, 85 ma. TDK EL0606 SKI-331K
Q1, Q2	MOSFET IRF840
Q3, Q5	MOSFET Supertex VP0104N3 P-channel 8 Ω
Q4, Q6	MOSFET Supertex VN1306N3 N-channel 8 Ω
R1	Thermistor NTC 3A Ametek SG220
R2, R3	Resistor 33 kΩ 5% 0.25W
R4, R5	500 Ω 10% 1W Corning FP1
R6	Thermistor PTC 3 kΩ Midwest 220Q32214
R8, R9	Resistor 100 kΩ 5% 0.25W
R10, R11	300 kΩ 5% 0.25W
R12	360 kΩ 1/2W 400V
R13, R18	3 kΩ 5% 0.25W
R14	17.4 kΩ 1% .25W
R15	240 Ω 5% 0.25W
R16	56 Ω 5% 0.25W
R17	10 k Ω 5% 0.25W
R19	9.31 kΩ 1% 0.25W
R20	1 MΩ 5% 0.25W
R21, R22	470 Ω 5% 0.25W
R23	910 Ω 5% 0.25W
R24	1 kΩ 5% 0.25W
R25	Trim pot. 200 Ω
R26	Resistor 20 k Ω 5% 0.25W
T1	PWR.Transformer. Core: Magnetics DF43622-UG. (1-2) = 12 turns of #30 AWG, six strands in parallel, split 6 turns + 6 turns. (3-4) = (4-5) = 1 turn of 0.005" copper foil, *sandwiched* between two halves of the primary (1-2). (6-7) = (7-8) = 3 turns of #30 AWG
T2	Transformer, current sense. Core: Magnetics 40705-TC-F (1-2) = 1 turn of #28 AWG (3-4) = 40 turns of #32 AWG
T3	Transformer, gate drive. Core: Magnetics 40705-TC-F. (1-2) = (3-4) = 20 turns of #32, double insulated wire, wound bifilar.
U1	Linear Regulator LM78M12
U2	FM Controller Gennum GP605
U3	Optocoupler Motorola MOC604A
U4	Shunt Regulator TI 431CLP

RMA 1

The GP605 in a Variable Frequency, Zero Current Switching, Forward Mode Resonant Mode Power Supply

APPLICATION NOTE

1.0 INTRODUCTION

Conventional quasi-square wave converters, mostly PWM controlled, have been very effective tools for power supply designers for quite a few years. Their most natural operating frequencies are between 20 kHz to 200 kHz. Lately,in the search to reduce size and cost, these converters are approaching the 500 kHz region, which is exotic for this topology. Recent developments in high frequency magnetics materials and high frequency capacitors make it possible to operate even in the high frequency region up to 1 MHz. This allows about a 3:1 reduction in the size of major passive components, as compared to 20 kHz switchers.

The biggest disadvantage for SMPS converters at these frequencies is high switching losses in power semiconductors. The resulting inefficiency requires larger heat sinks and thus defeats the goal of reducing the size.

There is, however, a more efficient way to convert power at ever higher frequencies. This class of converters is called "resonant" and can implement a zero current switching or zero voltage switching technique. A sinusoidal waveform can be generated either by a parallel or series resonating LC tank.

The clear advantage of the sine waveform is that switching generally occurs at zero crossing and switching losses in power semiconductors are almost eliminated or greatly reduced. The primary disadvantage of a resonant converter is that, for a given power level, the actual peak current is three to four times greater than that of a PWM converter. This can be overcome by using in some topologies fast SCR or, in general, by using low "on resistance" semiconductors. This creates a practical means to increase operating frequencies up to 1 MHz and higher. High frequencies allow designers to achieve power densities in excess of 25 W/cubic inch, which is about four times better than is possible at 100 kHz.

There are many types of resonant and quasi-resonant topologies. If you are interested in a brief review of some of these topologies, request the article published in IEEE Spectrum magazine, "*Resonant Mode Power Supply Design: A Primer*" by Fred Sykes , Gennum Corporation.

In this application note you will find a description of the zero current switching topology in variable frequency mode. An FM control type provides a fixed "*on time*" (T_{ON}),and variable frequency (f). Conversely PWM uses fixed period and variable on "*time*".

This paper describes features and applications of the GP605 resonant mode controller in one type of resonant power supply. The GP605 is an upgraded version of the LD405, which was the first commercially available resonant mode controller.

2.0 GP605 BLOCK DIAGRAM

Figure 1 shows a functional block diagram of the GP605. The heart of this IC is a voltage controlled oscillator (*VCO*) and a monostable. The *VCO* sets a variable commutating frequency, while the monostable sets a fixed T_{ON} time.

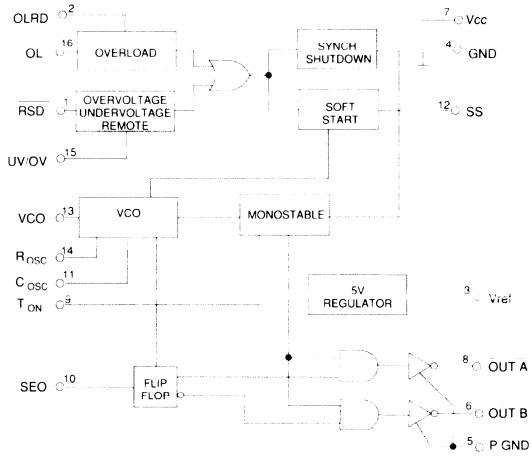


Fig. 1 GP605 Block Diagram

The IC can work either in a single-ended, or in a push-pull mode. Grounding pin 10 (*SEO*) enables a "*steering*" flip-flop to control the output AND gates, thus sending the drive to *OUT A* and *OUT B* in a push-pull mode. Opening pin 10 puts the chip into single-ended operation. In this mode the frequency is doubled compared to individual outputs in push-pull mode. The outputs are identical, so they can be paralleled for increased drive capability. T_{ON} time is independent of the mode of operation.

The chip has an overvoltage/undervoltage (*OVUV*) window comparator, the threshold of which can be set externally.

A soft-start block allows relatively slow frequency change, (usually measured in tens of milliseconds) from minimum *VCO* frequency to the value set by the *VCO* input pin 13. The soft-start initiates with every power-on of the chip, as well as after any forced shutdown.

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Shutdown can be achieved by grounding the remote shutdown pin 1 (*RSD*), by applying on pin 15 (*OVUV*) a voltage outside of the window comparator, or by applying a voltage level in excess of 3.2 V to the overload input pin 16 (*OL*).

Every shutdown of the GP605 is synchronous with the monostable, meaning that the controller never interrupts the T_{ON} in the middle of the pulse. This feature is especially suited for resonant power supplies, since resonant cycle interruption might cause excessive voltage spikes. These high dv/dt spikes could damage switching semiconductors, especially power MOSFETs. It is much safer to allow the cycle to elapse, and then to shut down the converter.

Every time the overload block shuts down the chip, it does so for 0.5 to 2 seconds resulting in a "*hiccup*" mode of overload protection. The exact timing is set by an external capacitor on pin 2 (*OLRD*). Such overload protection effectively "*folds back*" output on any prolonged overload or short. The converter will still have an automatic recovery once the voltage on *OL* pin drops below the threshold level.

3.0 RESONANT CIRCUIT THEORY OF OPERATION

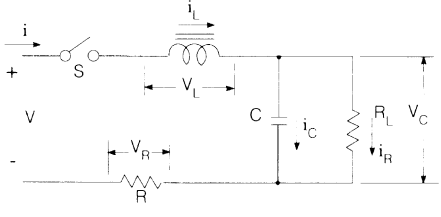


Fig. 2

In the circuit which consists of *L*, *C*, *R* and R_L there is a commutating switch *S*. Its function is to apply DC voltage of a known source *V* to a series resonating tank *LC*. Resistor R_L represents a load and "*steals*" some current from the tank. Once the resonant process is finished, the switch *S* is opened interrupting the power conversion from the source *V* to the resistor R_L. After a time interval, switch *S* is closed and the process repeats itself. One can change the commutating frequency, thus changing the average power being dissipated in the resistor R_L. If *L*, *C* and *S* were ideal components (which they are not), there would be no power dissipated anywhere, except into the load R_L and resistor *R*.

Let us first assume that $R_L = \infty$

$$i = i_L = i_C + i_R \qquad (1)$$

$$V = V_L + V_C + V_R = L\frac{di}{dt} + \frac{1}{C}\int i_C\,dt + i \bullet R \qquad (2)$$

The LC circuit has resonant conditions when:

$$X_L = X_C \qquad (3)$$

$$\text{i.e. } \omega L = \frac{1}{\omega C} \qquad (4)$$

Resonant frequency $\omega_O = 2\pi f_O$ can be determined from the expression:

$$\omega_O = \frac{1}{\sqrt{LC}} \qquad (5)$$

Impedance of resonating tank *Z* at the frequency ω_O:

$$Z = \omega_O L = \frac{1}{\omega_O C} = \sqrt{\frac{L}{C}} \qquad (6)$$

Ratio of reactive voltage V_L or V_C to the real voltage V_R, is called Quality factor *Q*:

$$Q = \frac{V_L}{V_R} = \frac{V_C}{V_R} = \frac{Z \bullet i}{R \bullet i} = \frac{Z}{R} \qquad (7)$$

Quality factor *Q* shows how many times voltage across inductor or across capacitor will exceed the source voltage *V*.
Let us determine the sum of the energy of magnetic and electric fields in the tank:

$$W = W_{mag} + W_{electric} \qquad (8)$$

current in the tank: $i = I_{peak} \bullet \sin \omega_O t \qquad (9)$

Then

$$V_C = V_{Cpeak} \bullet \sin\left(\omega_O t - \frac{\pi}{2}\right) = -V_{Cpeak} \cos \omega_O t \qquad (10)$$

$$W = W_{mag} + W_{electric} = \frac{L i^2}{2} + \frac{CV_C^2}{2}$$

$$= \frac{L I^2_{peak}}{2} \sin^2 \omega_O t + \frac{CV^2_{Cpeak}}{2} \cos^2 \omega_O t \qquad (11)$$

$$\text{But } V_{Cpeak} = \frac{1}{\omega_O C} \bullet I_{peak} = I_{peak}\sqrt{\frac{L}{C}} \qquad (12)$$

$$\text{So } \frac{CV^2_{Cpeak}}{2} = \frac{L I^2_{peak}}{2} \qquad (13)$$

$$\text{Then } W = W_{mag} + W_{electric} = \frac{L I^2_{peak}}{2} = \frac{CV^2_{Cpeak}}{2} = \text{const}$$

i.e. the sum of the magnetic fields does not change in time. The decrease in the electric field is compensated by the increase in the magnetic field and visa versa. Thus a constant conversion of the magnetic field into the electric field and back again is taking place.

The power dissipation takes place only in the resistor R. If the switch S is turned on for a period of time:

$$T_O = \frac{1}{\omega_O} = \frac{1}{2\pi f_O}$$

one complete resonant cycle will take place with power loss in the resistor R.

$$P = (I^2_{RMS}) \bullet R \qquad (14)$$

Differential equations for the circuit in Figure 2 are well known. The solutions are:

$$V_C = V + \frac{V}{\omega_O\sqrt{LC}} \bullet e^{-\frac{Rt}{2L}} \bullet \sin\left(\omega_O t + \frac{\pi}{2}\right) \qquad (15)$$

$$i = \frac{V}{\omega_O L} \bullet e^{-\frac{Rt}{2L}} \bullet \sin\left(\omega_O t\right) \qquad (16)$$

$$V_L = \frac{V}{-\omega_O\sqrt{LC}} \bullet e^{-\frac{Rt}{2L}} \bullet \sin\left(\omega_O t - \frac{\pi}{2}\right) \qquad (17)$$

The resulting waveforms are shown in Figure 3. Voltage V_C is circulating around the source voltage V. It cannot exceed V multiplied by 2. This voltage reaches its maximum point around $\frac{T_O}{2}$

The current is also circulating, although around zero.

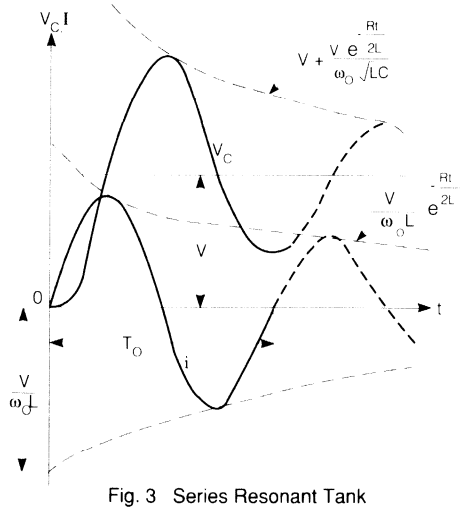


Fig. 3 Series Resonant Tank

For an ideal tank R = O

$$V_C = V - V\cos\omega_O t \qquad (18)$$

$$i = \frac{V}{\sqrt{L/C}}\sin\omega_O t \qquad (19)$$

$$V_L = V\cos\omega_O t \qquad (20)$$

This means that the resonating process would continue indefinitely. In the case of R_L being connected across capacitor C, the load will see an AC voltage V_C across it and thus will dissipate power. In practice, circuit R_L is connected to the tank via an isolation power transformer. The new value R_L' is then

$$R_L' = n^2 R_L, \text{ where } n = \frac{N_{pr}}{N_{sec}} \text{ is the turns ratio.}$$

4.0 RESONANT POWER SUPPLY

A block diagram of a parallel resonant converter is shown in Figure 4 . The detailed schematic diagram of this supply is shown in Figure 9.

An input circuit provides filtered DC bus voltage for the high frequency resonant converter. In the case described in this paper, the input circuit consists of input capacitors *C2, C3.*

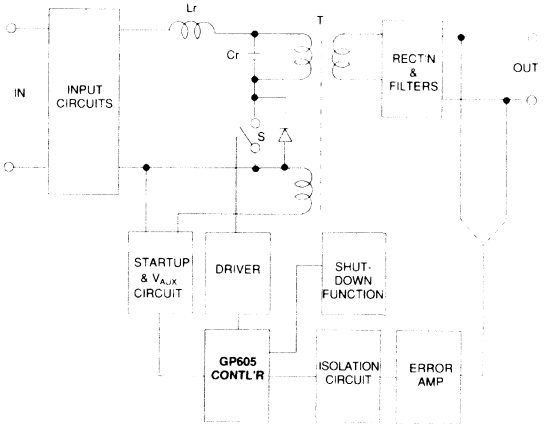


Fig. 4 Block Diagram of a Parallel Resonant Converter

The startup circuit provides energy for circuit operation at the time $T = 0$. Startup energy is supplied by current source *Q2.* The GP605 is in the OFF condition if voltage is below 9 V (typical). Once the power supply is up and running, energy is taken from the power transformer auxiliary winding *T2.*

The voltage from the winding is rectified (*CR8, CR7*) and regulated (*VR1*) to the level of 12 V. If the startup current is too high for your application please request the GP6040 data sheet 510-59. The GP6040 features very low startup current.

A resonating series tank consists of an inductor *L2* and capacitors *C4,C32.* The load is connected in parallel to the resonant capacitor via stepdown transformer *T2.* This type of converter, following old RF definition is called parallel resonant converters, despite the series resonant circuit.

The GP605 delivers constant "on" time to the switch and voltage regulation is achieved by frequency variation. Switch *Q1* is "on" for a period of time long enough for half of the full resonant cycle. A parallel diode to the switch provides a return path for the resonant current.

In order to provide fast turn-on and turn-off of the power switch Q1, driving requires an additional stage. This is achieved by using MOSFET transistors (*Q3, Q4*) in a totem-pole circuit configuration. Such an approach limits controller power dissipation and therefore increases product reliability.

The error amplifier in this particular application is designed on the secondary side. The error signal is transmitted to the primary via optocoupler *U2* and applied to the Voltage Control Oscillator (*VCO* input) pin 13.

The soft -start function is controlled by capacitor *C16* connected to pin 12. The controller of $T = 0$ applies minimum frequency to the circuit. The rate of frequency increase is controlled by capacitor *C16*. The frequency increases until it reaches the value set by the error amplifier.

The supply utilizes primary current sensing. Current sensing transformer *T1* is connected in series with the power transformer *T2*. The transformer has the turn ratio 1 : 50. On the secondary side the voltage signal is linearly proportional to the current on the primary side of the current transformer (*CT*). After rectification and some filtering, an essentially ""*saw tooth*" voltage level is applied to pin 16 of the controller. Once the signal reaches a programmed threshold, the controller shuts down for approximately 1 sec. The period is set by capacitor *C11* connected to pin 2. When time elapses the GP605 applies a normal pulse train, beginning from lowest frequency, as during soft-start function. If overload is still present the circuit goes to shutdown mode again. The supply will stay in the "*hiccup*" mode until the overload is removed.

The output stage is a fairly straightforward design. It is a full-wave Schottky, center-tap rectifier, composed of *CR10, CR11, L3* and a row of output capacitors.

5.0 DESIGN SEQUENCE

5.1 Integrating the GP605 in the Power Supply

5.1.1 Maximum and Minimum VCO Frequency ($f_{min/max}$)

The maximum operational frequency of the GP605 is 2 MHz. However usable frequency is limited by the *dead time* introduced internally to the end of each T_{ON} time, to prevent overlapping of the complementary outputs.

Since energy conversion takes place only during T_{ON} time, the limitation in D_{max} (duty cycle) lowers the practical maximum frequency (f_{max}). Table 1 gives useful information on T_{ON}, f_{max} and D_{max} for single-ended operation.

f_{max}	2000	1500	1000	600	500	400	kHz
T_{ON}	200	366	700	1366	100	2200	ns
D_{max}	40	55	70	82	85	88	%

Table 1.

If your application requires a high duty cycle in the 3 MHz frequency range, request GP6050, or GP6040 data sheets (documents 510-58 and 510-59 respectively, avail. Fall '89).

In this design f_{max}, is set at 510 kHz. A reasonable capacitor value from the noise point of view is 100 pF. For a 100 pF capacitor, from Figure 5 on GP605 data sheet, the minimum frequency is 12 kHz. From Figure 6 on the same data sheet, oscillator resistance is 26 kΩ.

Recommendations for oscillator components are:
- *C17* (oscillator capacitor) ceramic, temp. coef. NPO, 100 pF
- *R14* (oscillator resistance) metal film, 1%, 26.1 kΩ.

Tolerance of f_{max} from chip to chip is 5% (484 kHz to 536 kHz).

5.1.2 Set Output Pulse Width T_{ON}

The chosen resonant frequency is f_r = 600kHz. The T_{ON} pulse initiates the resonant cycle. The pulse must be terminated during conduction of the diode *CR3* (negative voltage on switch *Q1*). The best way to terminate the T_{ON} pulse is right in the middle of a negative half of the sinewave current:

$$T_{ON} = 0.75 \frac{1}{f_r}$$

From the above equation T_{ON} = 1250 ns. To limit the number of parts used in design, the value of the timing capacitor(*C18*) is equal to the oscillator capacitor, *C18* = 100 pF.

From Figure 2 on the GP605 data sheet (510-43) the timing resistor *R16* = 10 kΩ. A metal film, 1% resistor is recommended.

5.1.3 Soft-start Capacitor

This capacitor is connected to pin 12 and provides controlled startup from f_{min} to f_{max}. Startup requirements vary from application to application; for 100 W power level, a delay of 40 ms is chosen. The delay is approximately equal to:

$$T_{del}\ [\text{ms}] = 8.7 \times C\ [\mu\text{F}]$$

From the above, capacitor *C16* = 4.7μF

For a 500 W supply a delay time of 200 ms could be used.

5.1.4 VCO Input

In this design the *VCO* input voltage is set by an error amplifier via an optocoupler.

The proper level of the current in the photo transistor is set by an external resistor *R15* parallel to an internal 10 kΩ resistor. To achieve a *VCO* input level of 3.8 V (middle of the *VCO* range) *R15* = 3.9 kΩ.

5.1.5 Overload protection (OL)

Current sensing is provided by current transformer *T1*. Current on secondary side of the transformer is reduced by a factor of 50. After rectification and filtering, the voltage across capacitor *C13* is applied on pin 16. Once the level reaches 3.2V, the controller shuts down the power converter. The period of time the converter is shutdown is adjusted by capacitor *C11*. To achieve current limiting of 0.05 I_{max}, it is necessary to obtain restart every 1 s with additional 40 ms soft-start feature. From Figure 1 on the GP605 data sheet (510-43), *C11* = 4.7 µF and *R6* = *R7* = 300 kΩ (resistance on Figure 1 represents the parallel connection of *R6* and *R7*).

5.1.6 Driving Large Area MOSFETs

The GP605 is capable of delivering 0.6 A current in short pulses, but by using this feature it is very easy to exceed the maximum power dissipation of the package. Increased temperature of the chip will usually decrease reliability numbers. In this design the power MOSFET is driven by the totem pole small signal MOSFET stage *Q3*, *Q4*. The GP605 is driving only approximately 70pF load. Great care must be taken to prevent the voltage on the output pins from going below ground potential, or more than 0.5V above V_{CC}.

5.2 Power Transformer

Calculation of the power transformers for 500 kHz frequency range always causes a great challenge to the designer. The best choice is probably to use standard or custom made planar magnetics, whose electrical characteristics are best suited for a high frequency environment. Refer to (2) and (5) in the reference section.

If, for development purposes, it is required to design power magnetics for that high frequency, some useful information is presented in our application note 510-62 (Half Bridge Resonant Power Supply).

5.3 Resonating Tank

A very important part of the design is to choose the proper value of the resonant capacitor and resonant inductor. Too small an inductor creates high current peaks, too large an inductor leaves a small amount of power available for conversion.

A good starting point to choose the resonant tank capacitor is the output power estimation:

$$P_{OUT} = \frac{C_r \times V_{C\,peak}^2}{2} \times f$$

then

$$C_r = \frac{2 \times P_{OUT}}{V_{C\,peak}^2} \times \frac{1}{f}$$

$f = f_{max} = 510$ kHz

$P_{OUT} = 100$ W

$V_{Cpeak} = 72$ V

The calculated value of the capacitor is 0.0756 µF.

The iteration process to limit size, current peaks, and inductor size limits selected resonant capacitance to 0.044 µF.

The inductor can be calculated from equation

$$L_r = \frac{1}{C_r \times 4 \times \pi^2 \times f_r^2}$$

$f_r = 600$ kHz

Resonant inductor *L2* = 2.2 µH.

5.4 Power Semiconductor Selection

Used in this application the bilateral or fullwave switch consists of three major components, the MOSFET transistor *Q1*, the fast recovery diode *CR3* and the Schottky diode *CR1*. Transistor *Q1* is the main switching device and has a high requirement for maximum peak current. The Schottky diode *CR1* prevents the MOSFET parasitic diode from conducting (too slow for the purpose). The fast recovery diode *CR3* conducts to return resonant current.

Under maximum load condition the return current almost disappears and the peak current in the transistor can be cal culated from

$$I_{peak} = \frac{2 \times P_{IN}}{L_r \times f_{max}}$$

Peak current $I_{peak} = 14.7$ A

Then transistor RMS current

$$I_{RMS} = I_{peak} \sqrt{\frac{f_{max}}{4 \times f_r}}$$

RMS current $I_{RMS} = 6.8$ A

The power dissipation in resonant mode converters is limited mainly to conduction losses.

For IRFP250

$$P_{dt} = (I_{RMS})^2 \times R_t \quad (T_{amb} = 100\ ^\circ C)$$

$$P_{dt} = (6.8\ A)^2 \times 0.136 = 6.29\ W$$

The transistor requires very efficient cooling.

Schottky diode losses can be calculated from the following equation.

$$P_{SH} = I_{RMS} \times V_{RMS}$$

where

$$V_{RMS} = V_{peak} \sqrt{\frac{f_{max}}{4 \times f_r}}$$

Assuming $V_{peak} = 0.6$ V and $I_{RMS} = 6.8$ A, power dissipation on the Schottky diode is $P_{SH} = 1.89$ watts.

The return diode *CR3* conducts very little current at nominal load. Only at light loads will the diode conduct significant current, and then, the duty cycle is very low. The diode must be rated up to the transistor peak current. The power dissipation of this component is approximately 1 W. The total power dissipation for the bilateral switch is:

$$P_D = 6.29 + 1.89 + 1 = 9.18\ W$$

5.5 Snubbers

Snubber calculation is done as for a normal PWM converter.

The power loss on the resistor is

$$P_{PS} = \frac{C5 \times V_{max}}{2} \times f_{max}$$

$C5 = 680$ pF

$V_{max} = 100$ V

$f_{max} = 510$ kHz

The total snubber losses are $P_{PS} = 1.74$ watts.

5.6 Power Supply Efficiency

Power switch losses	9.2 watts
Output Schottky diode losses	11.0 watts
Losses in snubbers	1.8 watts
Control/drive circuits	0.5 watts
Power transformer losses (est)	2.0 watts
Output inductor dissipation (est)	2.0 watts
Resonating inductor dissipation (est)	0.5 watts
Miscellaneous losses	3.0 watts
TOTAL LOSSES	30.0 watts

$$\text{Estimated efficiency} = \frac{100\ W}{130\ W} \times 100\% = 78\ \%$$

Measured efficiency = 81 %

5.7 Possible Modifications to the Power Supply

This topology can be easily modified to achieve multiple outputs. Additional windings can be placed on the power transformer as long the total power does not exceed the rated value. If your application requires half bridge topology please request Application Note 510-62.

6.0 PERFORMANCE ANALYSIS

Efficiency	80%
Line regulation 36V to 60V	±0.1%
Load regulation 2A to 20A	±0.5%
Output ripple	33 mV

7.0 WAVEFORMS See next page

REFERENCES:

(1) Neville Mapham, "An SCR Inverter with Good Regulation and Sinewave Output", IEEE Trans. on Industry and General Applications Vol. IGA-3, pp. 176-187, March/April 1967.

(2) Alex Estrov, "Power Transformer Design for 1 MHz Resonant Converter", Proc. First High Frequency Power Conversion Conference, April 1987, Intertec Communications, Ventura, California.

(3) N.O. Sokal and A.D. Sokal, "Class E - a new class of high efficiency tuned, single-ended switching, power amplifiers", IEEE J. Solid-State Circuits, vol. SC-10, no. 3 pp. 168-176, June, 1975.

(4) Alex Estrov, Iain Scott, "FM Controller IC Supports up to 1 MHz Resonant Supplies", PCIM, Sept. 1987, Intertec Communications, Ventura, California.

(5) "The GP605 in a Variable Frequency, Zero Current Switching, Half Bridge, Resonant Power Supply", Gennum Corporation, Application Note 510-62

Fig. 5 Resonant Supply Waveforms

Upper trace: VDS 50V / div
Middle Trace: I_{TANK} 5A / div
Lower Trace: VGS 5V / div
at V_{IN} = 48 V
1 µs / div

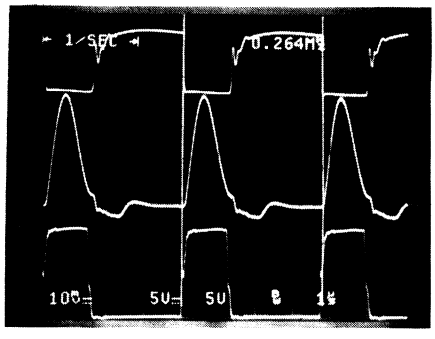


Fig. 5a. I_{OUT} = 20 A

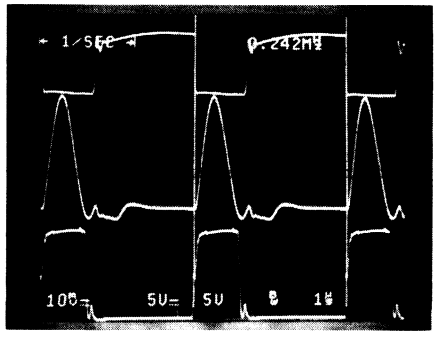


Fig. 5b. I_{OUT} = 15 A

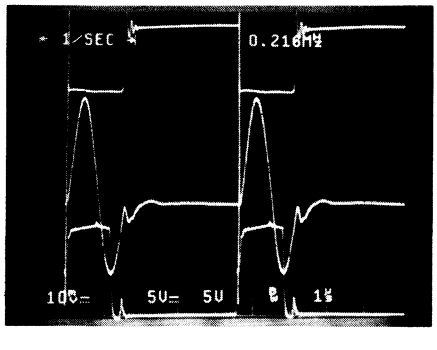


Fig. 5c. I_{OUT} = 5 A

Fig. 6 Resonant Supply Waveforms

Upper trace: VDS 50V / div
Middle Trace: I_{TANK} 5A / div
Lower Trace: VGS 5V / div
at I_{OUT} = 20 A
1 µs / div

Fig. 6a. V_{IN} = 36 V

Fig. 6b. V_{IN} = 40 V

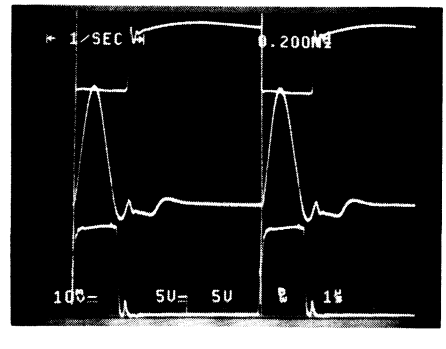


Fig. 6c. V_{IN} = 60 V

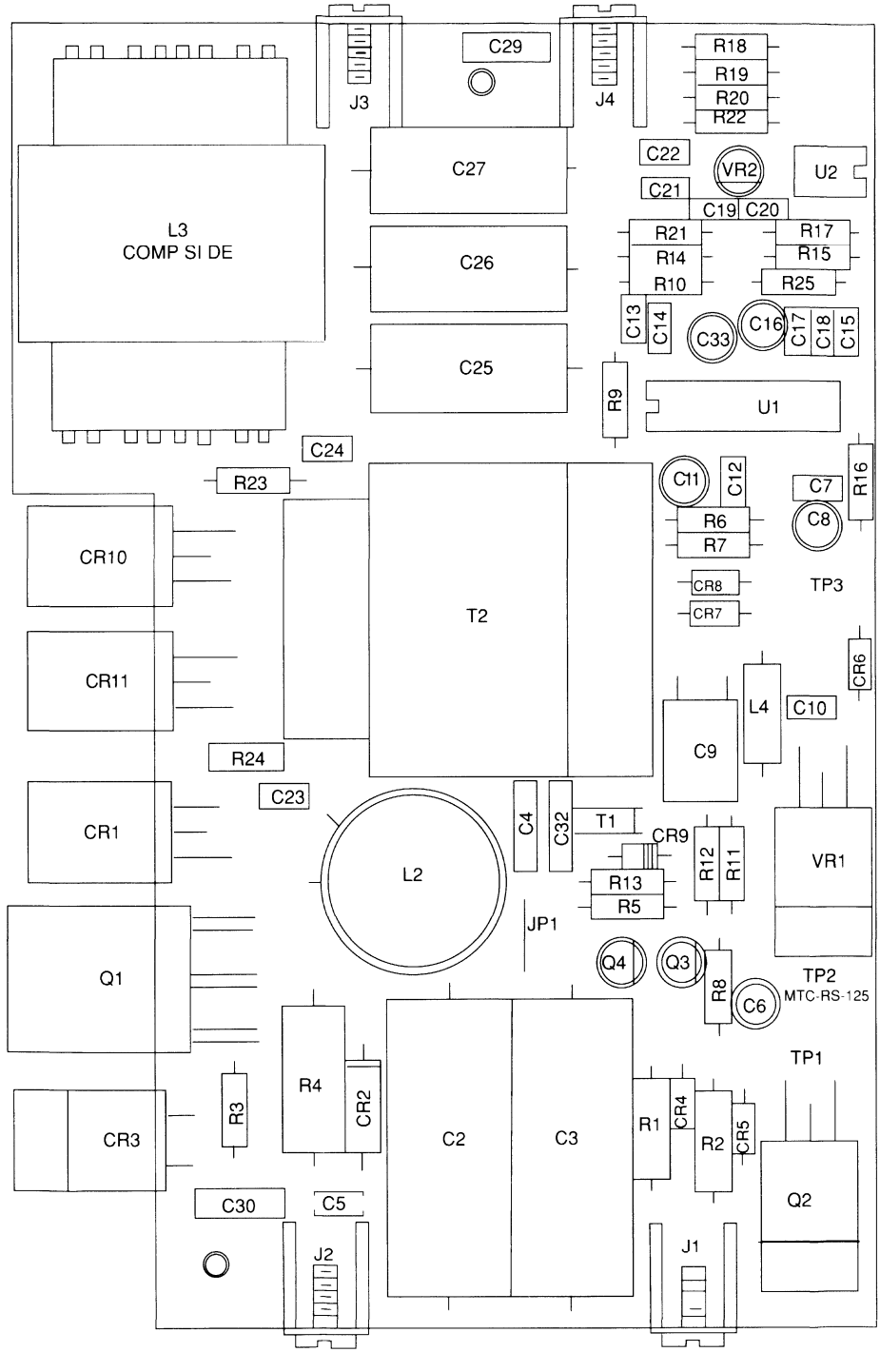


Fig. 7 PCB Layout of Resonant Converter 48V / 5V at 20 A

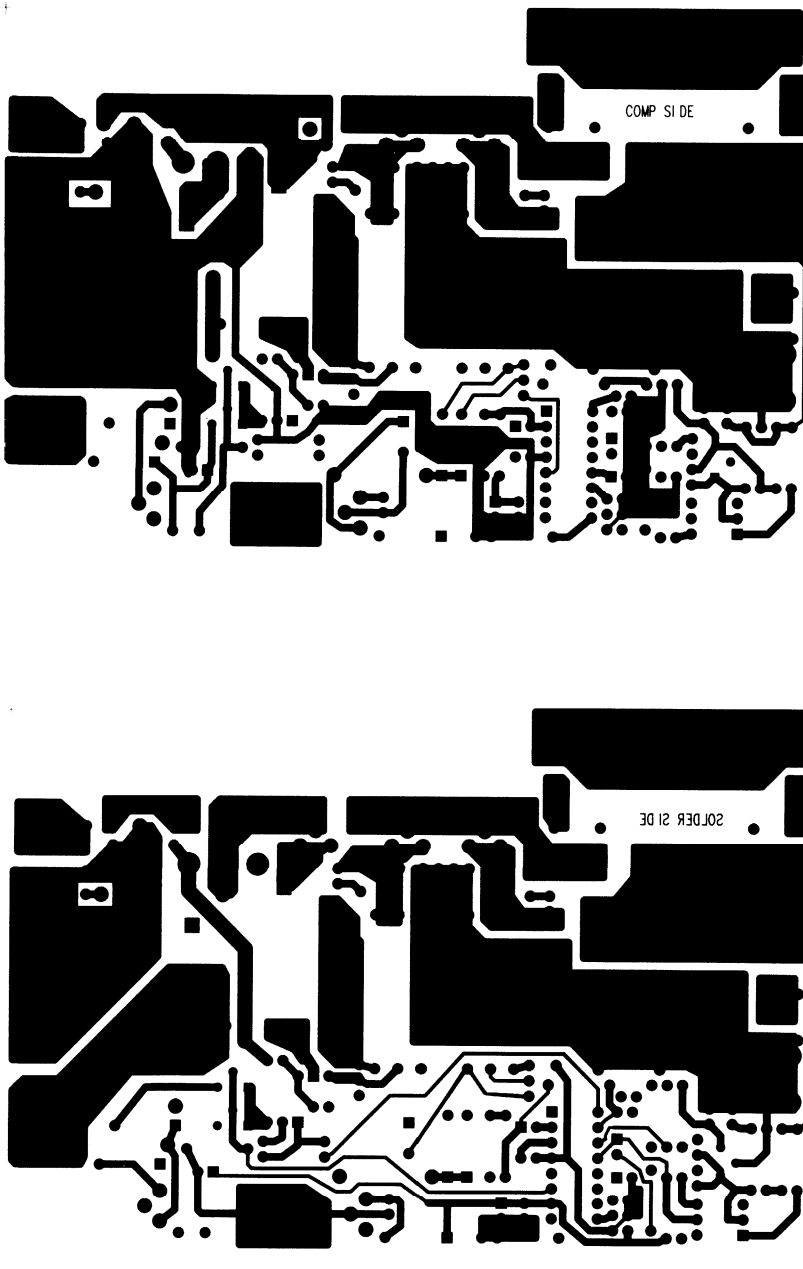


Fig. 8 Component and Solder Sides of the Resonant Converter 48V / 5V at 20 A

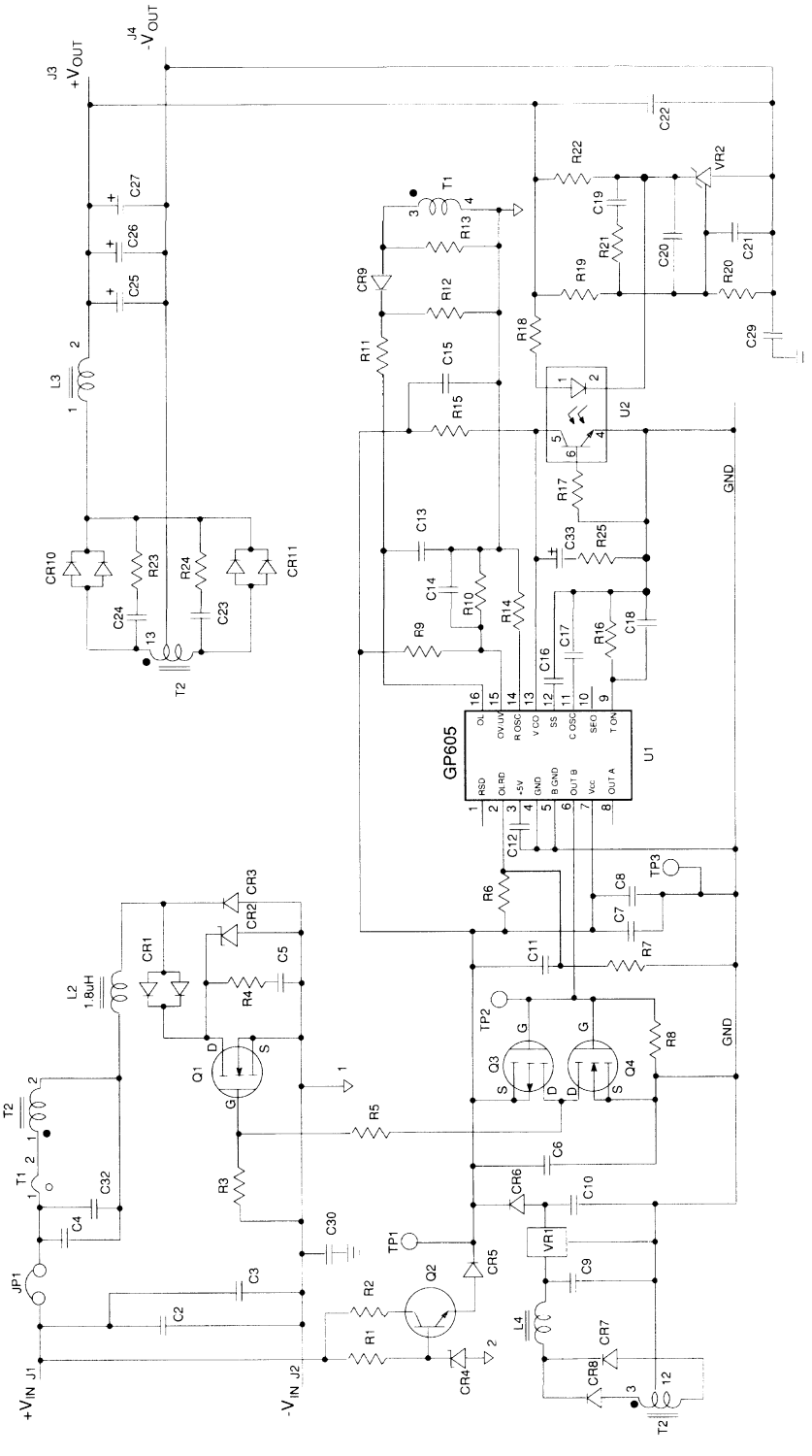


Fig. 9 Schematic of Resonant Converter 48V / 5V at 20 A

RESONANT MODE POWER SUPPLY
BILL OF MATERIAL

Part No.	Description
C2,C3	6.0µF 100V ±10% Electrocube 230BIB605k
C4,C32	0.022µF 200V NPO ±5% KEMET C340C223J2G5CA
C5	680pF 200V NPO (COG) ±5% KEMET C323C681J2G5CA
C6,C8	22µF 16V tant. dipped cap. Sprague 199D226X9016DA1
C7,C10,C15,C19,C20,C22	0.22µF 50V Z5U ±20% Sprague 1C10Z5U224M050B
C9	47µF 20V tant. dipped cap. Sprague 199D476X9020EE2
C11,C16,C33	4.7µF 16V tant. dipped cap. Sprague 199D475X9016BA1
C14,C21,C12	0.001µF 100V ±10% Sprague 1C10X5R102K100B
C13	0.022µF 50V ±20% Sprague 1C10Z5U223M050B
C17,C18	100pF 100V ±5% Sprague 1C10C0G101J050B
C23,C24	0.0022µF 100V C0G Sprague 1C10C0G222T050B
C25,C26,C27	220µF 10V 20% solid tantalum KEMET T262D227M010MS or CSR21C227KM
C29,C30	0.0022µF 500V CER. DISK Sprague 5TSD22 or 5GAD22
CR1	Schottky diode T0-220AB DUAL Amperex BYV4335 or Motorola MBR2035CT
CR2	Zener diode 170V ±10% 5W IN5385A
CR3	UFRD 15 A 200 V T0 220 AC Single Amperex BYV29-200 or Motorola MUR1520
CR4	Zener diode 12V ±5% 1/4W IN4699
CR5,CR6	IN4001 IA 50V
CR7,CR8	UFRD AXIAL 1A 200V Amperex BYV27-200 or Motorola MUR120
CR9	IN4148 Signal diode
CR10,CR11	Schottky diode T0-220, DUAL Motorola MBR2545CT or Amperex BYV 43-45
Q1	MOSFET IRFP250 International Rectifier T0-247AC
Q2	TIP 29C TI bipolar transistor
Q3	MOSFET VP0104N3 Supertex or Plessy ZVP2106A
Q4	MOSFET VN1306N3 Supertex or Plessy ZVN3306A
R1	180 Ω 1/2W 5%
R2	3.9 kΩ 1/2W 5%
R3,R8	51 kΩ 1/4W 5%
R4	47 Ω 3W 5% RCD RSF2B or Clarostat VC-3D

Part No.	Description
R5	2.2 Ω 1/4W 5%
R6,R7	300 kΩ 1/4W 5%
R9	3.6 kΩ 1/4W 5%
R10	1 kΩ 1/4W 5%
R11	220 Ω 1/4W 5%
R12	36 Ω 1/4W 5%
R13	22 kΩ 1/4W 5%
R14	26.1 kΩ 1% 1/4W
R15	3.9 kΩ 5% 1/4W
R16	10 kΩ 1% 1/4W
R17	1 MΩ 5% 1/4W
R18,R22	470 Ω 5% 1/4W
R19,R20	1 kΩ 1% 1/4W
R21	10 kΩ 5% 1/4W
R23,R24	51 Ω 1W 5% RCD RSF1A
R25	100 Ω 5% 1/4W
L2	2µH ±5% Core: T68-2D Micrometals 10 Turns #30 AWG x 5 (wire length = 10 inches)
L3	MTI-125-02-02 GAP=.012 Multisource Technology Inductor
L4	330µH 0.6 ohm Inductor AL0410-331K Northeastern Electronics (315)455-7561
T1	Current Sense Transformer: Primary: 1 turn #18 AWG Secondary: 50 turns #34 AWG Core: Ferroxcube 1041CT060/3E2A
T2	MTT-125-DC-06-02-06C Multisource Technology Transformer
VR1	LM7812 12V regulator
U1	GP605 Gennum Resonant Mode Controller
U2	CNY17-4 TRW Opto-coupler
VR2	TL431 CLP TI Shunt Regulator
MOUNTING HARDWARE	4 - 40 nuts and flathead bolts TO - 220 insulating bushings Bergquist insulators K4 - 90, K4 - 35 Washers for PCB spacing Baseplate Heatsink PCB Keystone #8190 terminals with screws

GENNUM CORPORATION

DC-DC Converter Kit - X485

INFORMATION NOTE

FEATURES

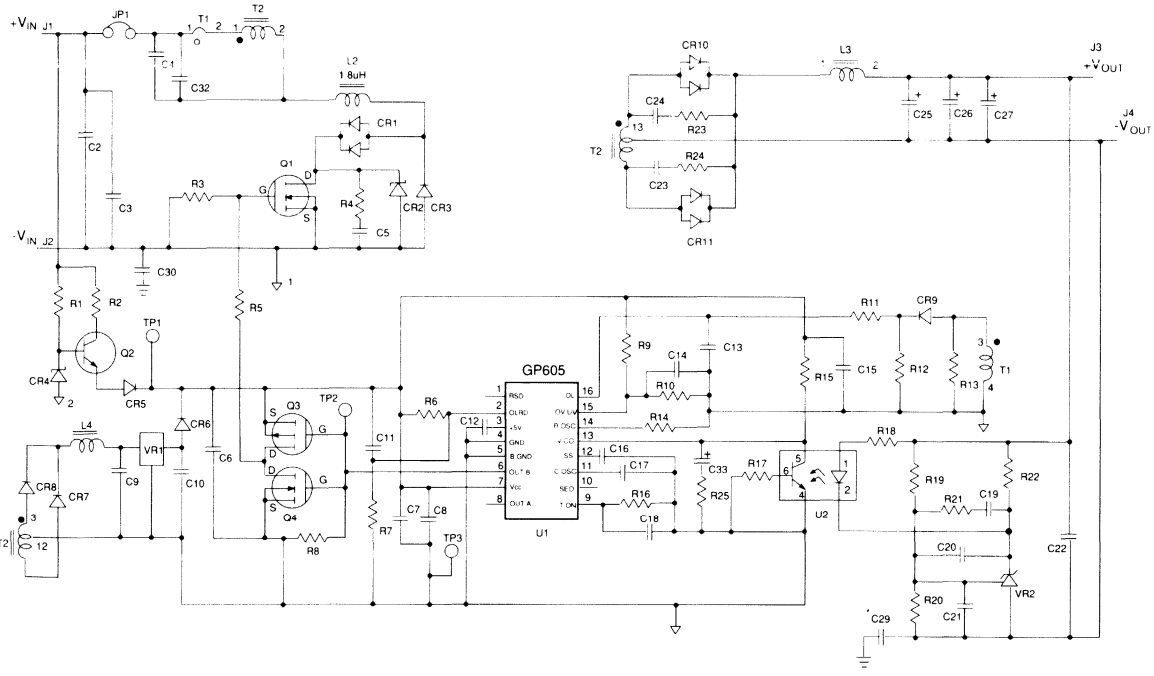
- small size 5.25" x 3.5" x 0.625"
- high power density
- lightweight
- small inductors and transformers
- 500 kHz switching frequency
- 100 W 5V output
- high efficiency 82%
- ideal for onboard power supply applications
- wide input range 36 V - 60 V DC
- overload protection
- short circuit protection

48V Input to 5V at 20 A Output, DC-DC Converter using the GP605 Resonant Mode Controller IC

This is a power supply kit being offered to demonstrate the potential of resonant mode as a control method for high performance power supplies.

The topology is based on a single-ended forward converter that has been converted to zero current switching by the introduction of a series resonant LC tank.

The GP605 resonant mode controller is a dedicated high performance controller that is used in this design. The GP605 provides the gate drive signal to the switching MOSFET. The GP605 generates fixed pulses at a varying frequency to regulate the output voltage. As well as providing the control, the GP605 also provides all the necessary peripheral functions such as Softstart, Undervoltage, Overvoltage and Overload Shutdown.



DC - DC Schematic

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

DC-DC Converter Kit

Specifications

Size 5.25" x 3.5" x 0.625"

Input voltage 36 VDC - 60 VDC

Output 5VDC at 20A

Efficiency 80%

Line Regulation ±0.1%

Load Regulation ±0.5%

Output Ripple 50 mVpp

Kit Components

To eliminate any problems associated with resonant mode evaluation, the DC-DC Converter Kit is a complete power supply provided in unassembled form. The kit is comprised of all necessary components including the PCB, heatsink, and backplate.

To simplify the assembly and testing, a manual is also provided showing how to assemble the power supply, and how to test for proper operation. All the major waveforms are provided for comparison.

For information on the theory and development of an original design ask for the Gennum Application Note 510-63, *The GP605 in Variable Frequency Zero Current Switching, Forward Mode, Resonant Power Supply*.

This reprint from POWERCONVERSION & INTELLIGENT MOTION magazine, September '87, is courtesy of GENNUM CORPORATION

FM Controller IC Supports up to 1 MHz Resonant Supplies

A new FM controller IC for use with resonant supplies provides regulation, soft-start, undervoltage/overvoltage shutdown, overload current limit, remote shutdown and direct drive for output switches. An example of resonant converter using the controller is detailed.

by
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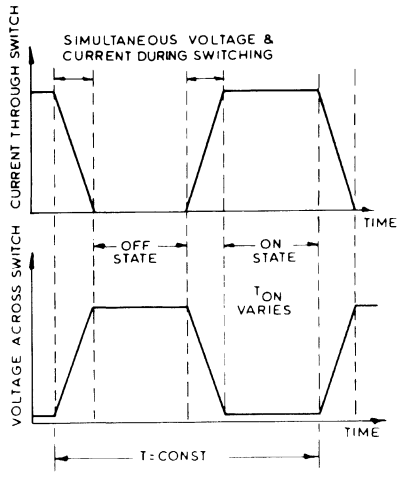
Most resonant and quasi-resonant topology power supplies employ frequency modulation (FM) control that provides a fixed pulse width and variable period. These supplies can be simplified by use of the LD405 FM controller, the first IC specifically intended for frequency-modulated resonant supplies.

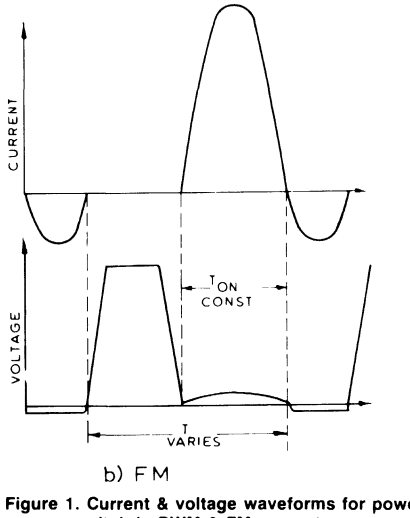
Resonant Converters

Resonant converters are an efficient technique for converting power at higher frequencies. They use "zero current" or "sine wave" current switching (*Figure 1*) generated by either a parallel or series resonating LC tank circuit.

The advantage of sine wave current is that transistor switching generally occurs at zero current, which practically eliminates switching losses in power semiconductors. The primary disadvantage of a resonant converter is that for a given power, the actual peak current is three to four times greater than that of a PWM converter. This can be overcome by using lower ON resistance



a) PWM



b) FM

Figure 1. Current & voltage waveforms for power switch in PWM & FM converters.

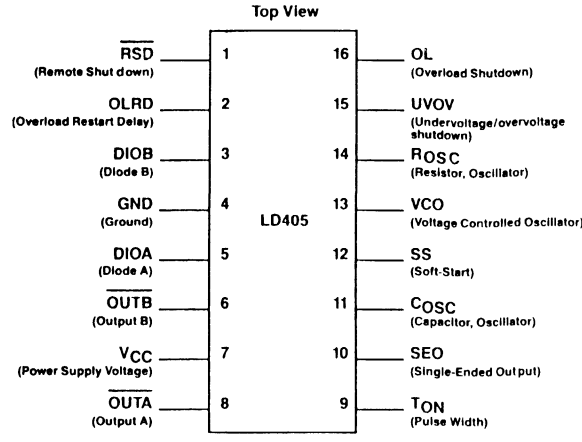


Figure 3. Connection diagram.

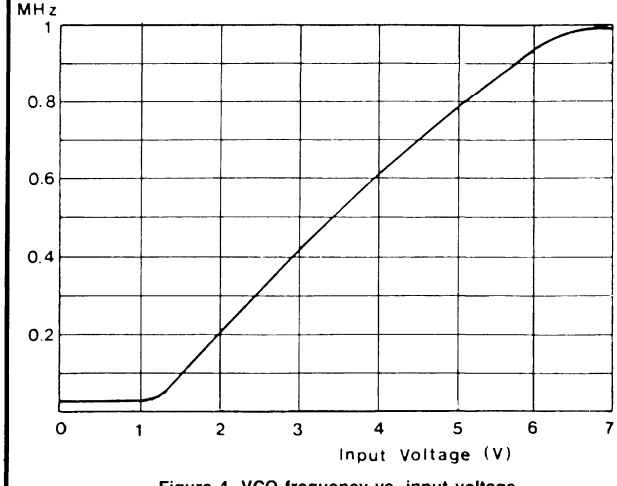


Figure 4. VCO frequency vs. input voltage.

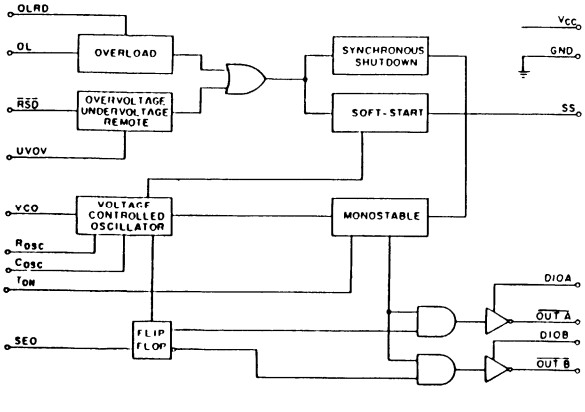


Figure 2. Functional block diagram.

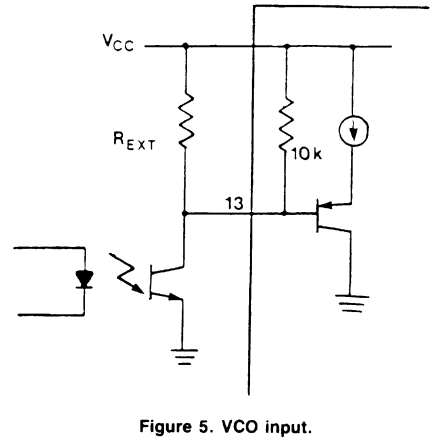


Figure 5. VCO input.

semiconductors, so the technique allows operating frequencies above 1MHz. These frequencies allow designers to achieve power densities more than 25W/in^3, which is about four times better than a 100kHz converter.

A block diagram of the LD405 and its pinouts are shown in *Figures 2* and *3*, respectively. At the heart of this device is a high stability, voltage-controlled oscillator (VCO) and a monostable multivibrator. These two circuits control the pulse width and operating frequency of the output drivers.

A resistor and capacitor at pin 9 sets the fixed pulse width, T_{ON} of the monostable. The VCO is intended for an optocoupler (*Figure 4*), or any other type of feedback network from the secondary (output) side of the power supply. Its control characteristic (*Figure 5*) is linear within ±5% over the range of 1.5V (f_{MIN}) to 6.5V (f_{MAX}). A capacitor on pin 11 (C_{OSC}) sets f_{MIN}. After selecting the capacitor, a resistor on pin 14 ($_{OSC}$) sets f_{MAX}.

The three shutdown modes are Remote Shutdown (RSD) on pin 1, Undervoltage/Overvoltage Shutdown (UVOV) on pin 15 and Overload Shutdown (OL) on pin 16. Every shutdown is synchronous with the monostable and the controller never interrupts the output pulse. This feature is well-suited for resonant supplies because resonant cycle interruption might cause excessive voltage spikes that can damage switching semiconductors, particularly power MOSFETs. It is much safer to allow the cycle to finish and then shut down the converter for a relatively long time.

The soft-start block allows a slow (usually tens of milliseconds) change from minimum VCO frequency to the value set by the VCO input voltage. A capacitor on pin 12 (SS) controls the soft-start delay, which is triggered at power-on and after any forced shutdown. To achieve shutdown, ground the remote shutdown (RSD) pin 1, apply a voltage greater than 3.2V to pin 16 (OL), or apply less than 1.8V or more than 3.2V to UVOV (pin 15).

Overload shutdown starts the Overload Restart Delay (OLRD, pin 2), which lasts for 0.5 to 2 sec, depending on the capacitor value at pin 2. This overload protection method effectively folds back the output for a prolonged overload. Once the voltage on the OL pin drops below its threshold, the converter automatically recovers.

Push-pull outputs $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ are capable on driving power MOSFETs. $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ both require external anti-saturation diodes, which can be 1N914s of their equivalents.

The LD405 can operate either single-ended or push-pull. Grounding SEO (pin 10) causes push-pull operation and opening pin 10 provides single-ended operation at twice the push-pull frequency. Both outputs are identical, allowing parallel operation for increased drive capability. The pulse width, T_{ON}, is independent of the operating mode.

Design example

An example of an off-line resonant supply is shown in the block diagram of *Figure 6* and its schematic in *Figure 7*.

The rectifier/voltage doubler block provides an unregulated 300VDC (VNR) bus for the high frequency resonant converter. The resonating tank consists of inductor L1 and capacitor C7 connected in series. Power transformer T1 accepts the sinusoidal voltage across C7 and steps it down to the output stage.

In terms of its driving sequence, this resonant converter operates in a manner similar to a half-bridge square wave converter. The resonating cycle involves switch Q1, the parallel combination of C7 and the primary winding of T1, inductor L1 and one turn of current sense transformer T2. Return current flows via diode D4 and capacitor C1 is a voltage source for the resonating cycle. Initially, switch Q1 is ON and switch Q2 is OFF.

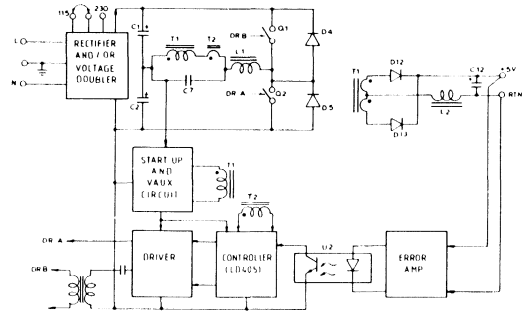


Figure 6. Resonant power supply block diagram.

Except for using switch Q2 instead of Q1, the second resonating cycle involves the same components as the first cycle. Return current flows through diode D5 and capacitor C2 is a voltage source for the second cycle. Note that current reverses its polarity in the second cycle (compared with the first cycle), so T1 operates in a bipolar mode. During the time Q2 is OFF, D4 clamps the voltage across Q2 to the level of the VNR bus. D5 does the same for Q1.

Q1, Q2, D4 and D5 need a rating of only 420V because the line voltage (132V or 264Vrms) after rectifying and doubling allows then a 50V safety margin.

The 5VDC, 25A output stage is straightforward, using a full-wave, center-tapped Schottky diode bridge consisting of D12, D13, L2 and C12.

Regulation

Changing the commutation frequency of the LD405 controller provides regulation. Its VCO receives the input signal from an error amplifier via optical coupler U2. The controller performs the functions previously described: soft-start, overload current limit, VNR bus undervoltage and overvoltage shutdown, and remote shutdown.

An additional driver stage consisting of Q3, Q4, Q5 and Q6 and transformer T3 provides faster turn ON and OFF for power MOSFET switches Q1 and Q2. The average power to drive both switches is under 1W, but the switches require short duration pulses up to 0.75A to charge and discharge the gate-source capacitance.

The 12VDC VAUX bus powers the LD405 and the drivers. C2, via limiting resistor R6, transistor Q7 and diode D6 provide this voltage during start-up. Zener diode, D15, holds Q7's base at a constant 12V during start-up, providing about 10.6V to the VAUX bus. Winding 6-8 of T1 provides the voltage source for the VAUX bus when the supply is running, usually about 20msec after start-up. D8 and D9 rectify the voltage from this winding and U1 regulates it to 12V ±5%. After start-up, D6 is reverse-biased, which prevents power loss from Q7 and R6.

The primary of power transformer T1 is in series with the single-turn winding of current-sensing transformer T2. T2 has a turns ratio of 1:40 and its secondary winding voltage is linearly proportional to the primary winding current. These voltage pulses mirror the current pulses in the primary of T1.

Diodes, capacitors and resistors rectify and filter the output of T2's secondary, providing a sawtooth voltage to OL (pin 16 of the LD405) that is proportional to the total load. Upon reaching its threshold, the LD405 shuts down for about 1 sec, as determined by the 4.7mF tantalum

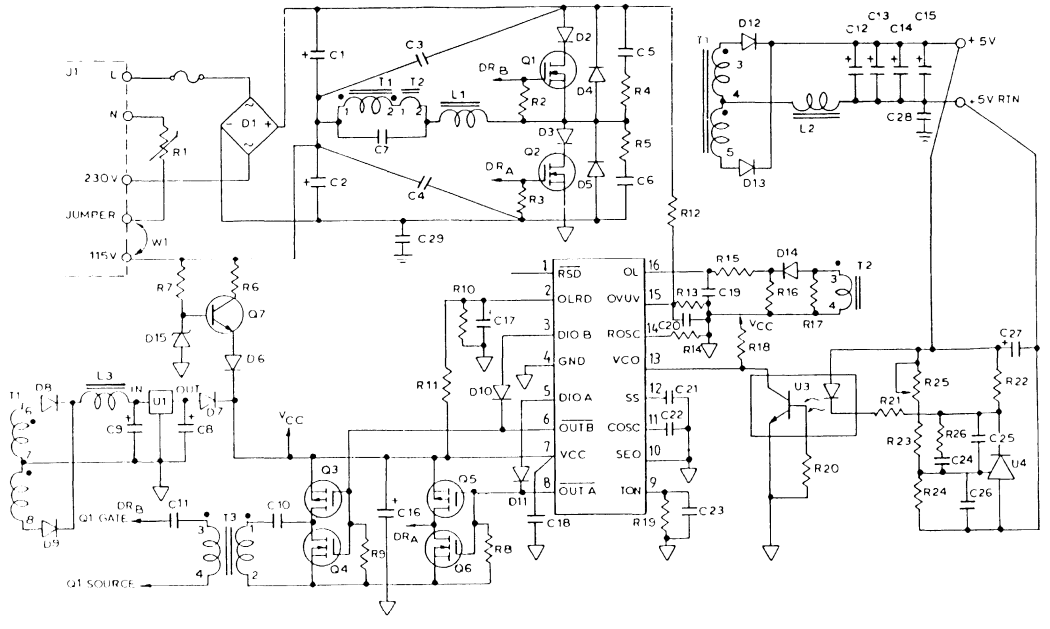
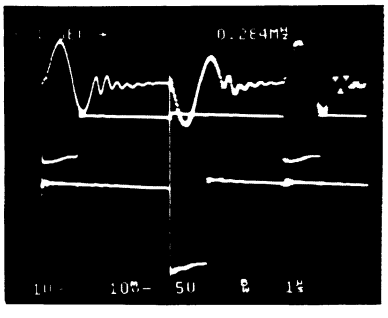


Figure 7. Resonant off line power supply schematic.

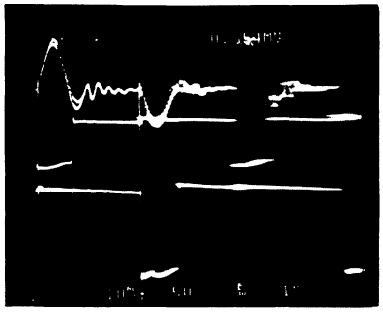


8a) 50 watts, 115VAC

5A/division

10V/division $\overline{OUTA}$

5V/division $\overline{OUTB}$



8b) 125 watts, 100VAC

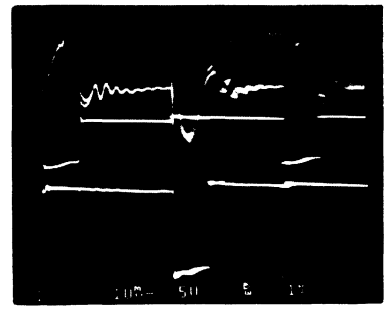
5A/division

10V/division $\overline{OUTA}$

5V/division $\overline{OUTB}$

capacitor connected to pin 2. When this period has elapsed, the controller starts generating its pulse train. The frequency of these pulses is initially about 10kHz (f_{MIN}) and increases according to a preset time constant. In about 20 msec, if the overload condition continues, it shuts down again. The supply stays in this "hiccup" mode until removal of the overload.

The maximum commutation frequency (f_{MAX}) of the supply is 600kHz. C7 is 8200pF and L1 is 5mH, therefore the resonant frequency is about 750kHz. T1's primary inductance is at least 100 times higher than that of L1, so it does not affect the resonant frequency of C7-L1. *Figure 8* shows current waveforms in L1 vs the outputs of the LD405 at different load and line levels. Only the first pulses appear to be in focus because the controller constantly changes the commutating frequency to reject input AC line ripple.



8c) 125 watts, 132VAC

5A/division

10V/division $\overline{OUTA}$

5V/division $\overline{OUTB}$

Figure 8.

SPECIAL APPLICATION PRODUCTS

SPD

data sheets

Gennum engineers and others
in our Marketing Department
are always available to discuss
any proprietary design/custom product
requirements you may have.
Please ask for our brochure BR508

GENNUM CORPORATION

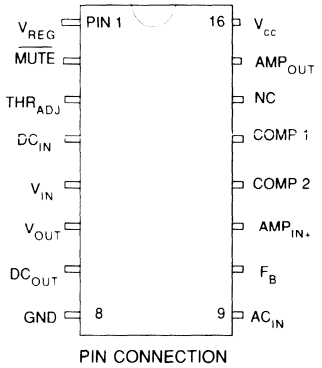
High Performance AGC Amplifier

LC403, LD403 DATA SHEET

FEATURES

- high stability of output level
- 40 dB AGC operating range
- adjustable AGC threshold
- adjustable attack and release time
- levels adjustable with external components
- can be operated as a voltage controlled gain amplifier
- two gain blocks may be used separately
- maximum frequency 100 kHz
- threshold detector (squelch option)
- operates from standard 5V power supply
- industrial or military temperature range

TOP VIEW



PIN CONNECTION
16 PIN DIP

Part No.	16 Pin Package	Temperature Range
LC403D	PLASTIC	-25°C TO +85°C
LD403D	CERAMIC	-55°C TO +125°C MIL 883B screened

ORDERING INFORMATION

INTRODUCTION

The LC/LD403 can be divided into three functional blocks plus a voltage regulator. The voltage regulator takes the power supply voltage of 5 V to 10 V and regulates it down to 3.65 V for internal use. It is also brought out on Pin 1 for decoupling and external applications. Up to 1mA may be drawn from it. The three functional blocks are the output amplifier, attenuator-preamplifier, and the automatic gain control section. Refer to Figure 1.

BLOCK DIAGRAM

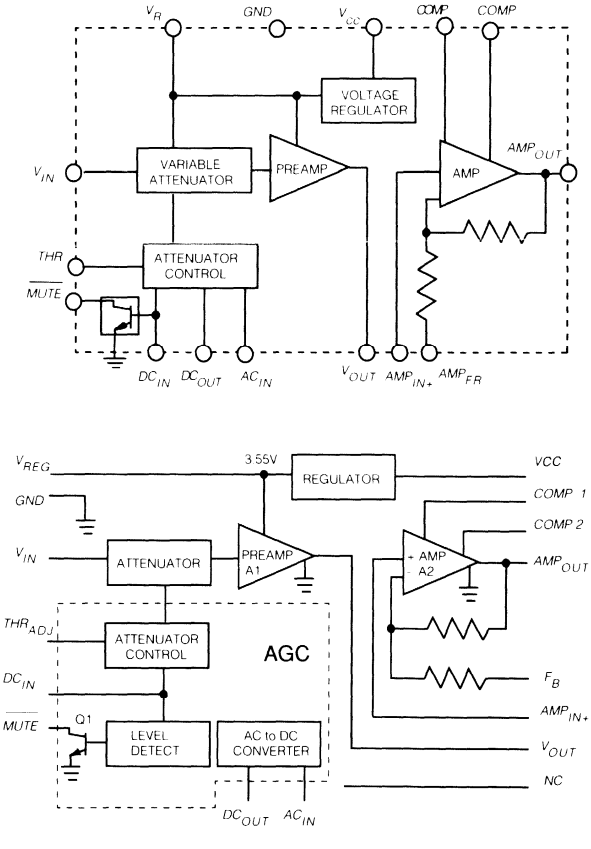


Fig.1 Functional Block Diagram

SPD 1

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DESCRIPTION

Amplifier

The main amplifier is brought out on five pins as a separate component. COMP1, COMP2 are intended for a nominal 150 pF capacitor, which gives a bandwidth of 500 kHz. Access is provided to the non-inverting input (AMP_{IN+}) and the internal feedback network (*FB*). The gain is set at 18dB but this may be modified using the feedback pin *FB*.

The output stage of the amplifier is designed to drive a 600 Ω load to 2.3 Vpp (maximum), and can be biased by directly connecting the preamplifier output to the non-inverting amplifier input. This internal bias level is optimised for V_{CC} = 5 volts. The amplifier operates off V_{CC} and when V_{CC} > 5 volts, it may be advantageous to bias the input externally in order to obtain increased output voltage and symmetrical clipping. The optimum bias voltage versus V_{CC} is

$$\frac{V_{CC}}{2} \quad -0.5\ V$$

A capacitor will be necessary between the preamplifier output and amplifier input for DC isolation.

Attenuator-Preamplifier

The input signal to the attenuator (V_{IN}) must be connected through a capacitor. A direct connection will disturb the internal bias levels of the LC403. The attenuator is driven by the automatic gain control (AGC) circuit. The gain of the preamplifier is +24 dB and the output is connected to the AC to DC converter through a capacitor. Because of current drive limitations, the minimum load resistance on the output of the preamplifier is 10 kΩ

AGC Section

When the signal at the input of the AC to DC converter (AC_{IN}) exceeds a reference threshold, both positive and negative peaks charge the AGC capacitor *C*.

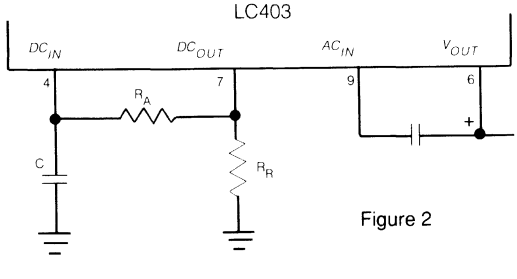


Figure 2

The DC voltage developed on this capacitor is applied to the attenuator control circuit at DC_{IN}, which varies the attenuation to maintain the input signal to the preamplifier at a constant level. For performance and stability reasons, this capacitor must be at least 2.2 µF (minimum). The attack and release time constants are determined by R_A and R_R together with *C*. The minimum value for R_R is 1 MΩ.

OPERATING MODES

The AGC threshold is set by a resistor (R_T) on pin 3 (THR_{ADJ}). A lower threshold represents higher initial gain, ie the attenuator-preamplifier reference gain setting is controlled by R_T. Refer to Figure 12, R_T vs AGC Threshold V_T and Figure 11, AGC Characteristic.

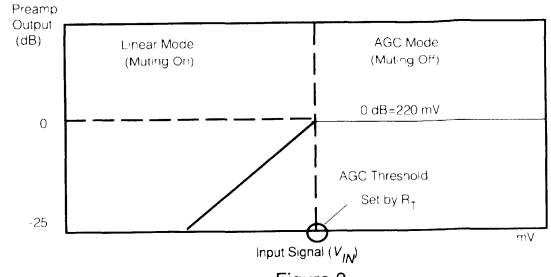


Figure 3

At input levels less than the threshold, the attenuator and preamplifier operate in a linear mode with fixed gain. This gain is determined by R_T. Alternatively, a voltage can be applied at pin 4 (ATT_{IN}) to control the gain (refer to Fig. 13 Attenuation Function of DC Control Voltage). When the input reaches and exceeds the AGC threshold, attenuation is increased to maintain the preamplifier output at a constant level. The attenuator and preamplifier are now operating in the AGC mode. As the input varies, the attenuation tracks it with attack and release time constants set by R_A, R_R and *C*.

A Cautionary Note

The resistor R_T sets up a current given by:

$$I_T = \frac{V_{CC} - 1.2\ V}{R_T + 5\ k\Omega}$$

This current is used to set the AGC threshold. V_{CC} must be well regulated and decoupled as close to the chip as possible.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage V_{CC}	10 V
Input Signal V_{IN}	4 Vpp(capacitive coupled)
Attenuator Control Input DC_{IN}	0.3 V to +3.5 V
Amplifier Input AMP_{IN+}	0.3 V to V_{CC} + 0.3 V
Operating Temperature Range:	
LC403D	-25°C to +85°C
LD403D	-55°C to +125°C
Storage Temperature Range	-65°C ≤T_S ≤ 150°C
Lead Temperature (Soldering 10 sec)	260°C
Junction Temperature	150°C
Power Dissipation	(at T_A = 25°C) 500 mW

ELECTRICAL CHARACTERISTICS

Limits apply over -25°C ≤ T_A ≤+85°C for the LC403 and -55°C ≤ T_A ≤ +125°C for the LD403. V_{CC} = 5V. Typical values are at T_A = 25°C. Parameters marked with a * are valid only at T_A = 25°C. The test circuit is shown in Figure 4.

SECTION	PARAMETER	CONDITIONS / NOTES	MIN	TYP	MAX	UNITS
General	V_{CC}	Supply Voltage	4.75	5.0	10.0	V
	I_{CC}	Supply Current, No Signal	-	12	16	mA
	V_{REG}	Regulated Output*	3.47	3.65	3.85	V
		Temperature Coefficient of V_{REG}*	-	100	-	ppm/°C
	I_{REG}	Max Output Current for V_{REG}	-	-	3	mA
	C_{REG}	Decoupling Capacitor for V_{REG}	4.7	-	-	µF
	C_S	Power Supply Decoupling Capacitor	10	-	-	µF
	S / N	Signal To Noise Ratio at Amplifier Output with V_{IN} = 200mVpp at 1kHz AGC Mode, 300Hz -10kHz	-	65	-	dB
	THD	At Amplifier Output For V_{IN} = 100 -1000 mVpp at 1kHz	-	0.3	-	%
Amplifier	A2	Amplifier Gain with Internal Resistors	17	18	20	dB
		Temp Coefficient Of Amplifier Gain	-	-	500	ppm/°C
	$Z_{IN\ 2}$	Amplifier Input Impedance	10k	-	-	kΩ
	$Z_{OUT\ 2}$	Amplifier Output Impedance at 1 kHz	-	-	10	Ω
	Clipping Voltage	600 Ω Load Internal Bias	-	3	-	Vpp
		2 kΩ Load External Bias	-	Vcc-1	-	Vpp
	Slew Rate	600 Ω Load	-	3	-	V/µs
	Input Bias	AMP_{IN+}	1	2	4	µA
	Output	Source	20	-	-	mA
	Current	Sink	5	-	-	mA
	TCR	Feedback Resistor Temp Coefficient	-	2000	-	ppm/°C
	Bandwidth	at -3 dB C_C = 150 pF	-	0.5	-	MHz
Attenuator/ Preamplifier	V_{IN}	Attenuator Input at 1 kHz, 0.3 % THD, AGC Threshold = 20 mV pp	-	-	1000	mVpp
	V_{OUT}	Preamp Output In AGC Mode Minimum 10 kΩ Load*	180	230	280	mVpp
	A1	Preamp Gain in Linear Mode	-	24	-	dB
	$Z_{IN\ 1}$	Attenuator Input Impedance at 1kHz	10	-	-	kΩ
	$Z_{OUT\ 1}$	Preamp Output Impedance at 1kHz	-	20	-	Ω
	Clipping Voltage	V_{OUT} (10 kΩ Load)		0.8	-	Vpp
	Slew Rate	V_{OUT} (10 kΩ Load)	-	1.5	-	V/µs
	Bias Level	Preamp Output DC Bias Level No Signal	-	2.1	-	V
	R_S	Source Impedance for V_{IN}	-	-	5	kΩ
	Attenuation Range	Not Including Preamp Gain	2	-	40	dB
	Output	Source	3	-	-	mA
	Current	Sink	0.5	-	-	mA
	ΔV_{OUT}	Preamp Output Level Shift with Input Level Change V_{IN} = 20 to 1000 mV pp	-	0.2	-	dB

continued over

ELECTRICAL CHARACTERISTICS continued

SECTION	PARAMETER	CONDITIONS / NOTES	MIN	TYP	MAX	UNITS
AGC	Z_{IN3}	AC to DC Converter Input Impedance (AC_{IN})	5	-	-	kΩ
	Z_{IN4}	Attenuator Control Input Impedance (DC_{IN})	-	2000	-	kΩ
	C	Attack / Release Time Constant Capacitor	-	2.2	-	µF
	R_A	Attack Time Constant Resistor	0	-	10	kΩ
	R_R	Release Time Constant Resistor	0.5	1	4.7	MΩ
	V	AGC Threshold $R_T = \infty$	-	20	-	mV pp
	Q1	Muting Transistor Sink Current	-	-	1	mA

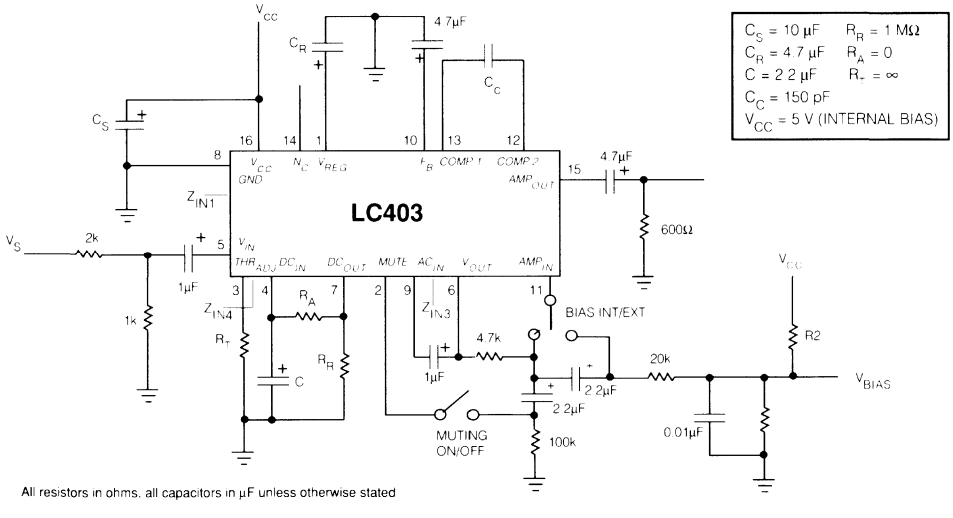


Fig.4 Test Circuit

APPLICATIONS

The circuit in Figure 5 represents an application for minimal external components. There is no provision for adjusting the output level or the input signal range. The attack time is set at minimum; however the release time can be controlled by selecting proper values for C and R_R.

The circuit in Figure 6 provides more flexibility in selecting levels. The input signal range, nominally 7 to 350 mV RMS can be shifted towards higher levels with the attenuator *R1* and *R2*. The combination of *R1* and *R2* can also be used for matching the source impedance, where necessary. The output level can be reduced by up to 8 dB with the potentiometer. The input threshold is not affected. The attack time can be reduced with R_A. The threshold can be adjusted with R_T. The muting feature is obtained by *R3*, *C1* and *R4*.

When the input signal is under the threshold the mute pin is pulled down and *C1* shorts the AC signals to ground, cutting off the noise when there is no input signal or the input signal is too low to be useful. The level at which the muting operates can be adjusted by selecting the proper value for R_T.

The circuit in Figure 7 offers a few extra features. The amplifier input is biased from the power supply voltage. This will permit higher output levels when the power supply voltage is more than 5 volts. The AGC signal is taken from the amplifier output rather than from the preamplifier. Resistor, *R5* controls the output level, but in this case the AGC threshold is also affected. With this configuration, the total harmonic distortion can be reduced to 0.1%.

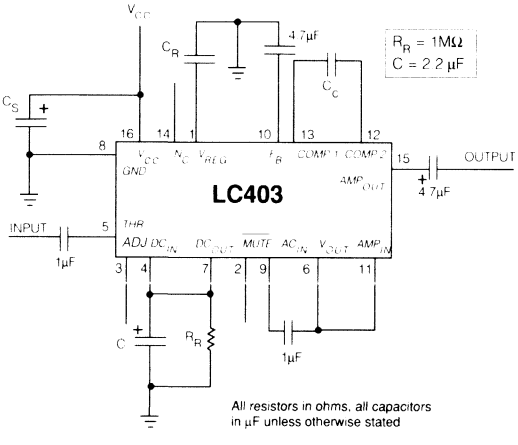


Fig.5 Minimum Components

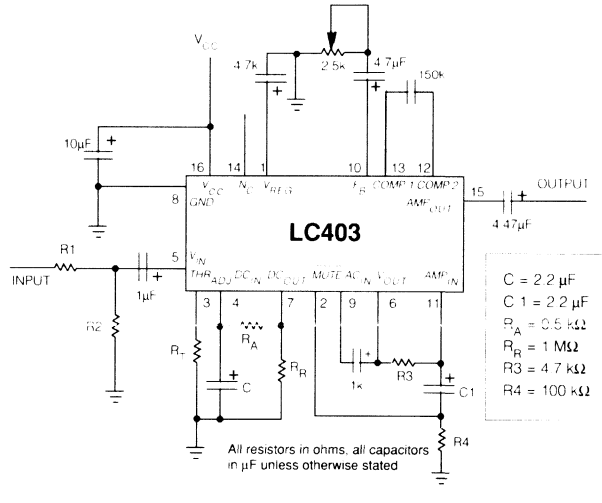


Fig.6 Adjustable Characteristics with Muting

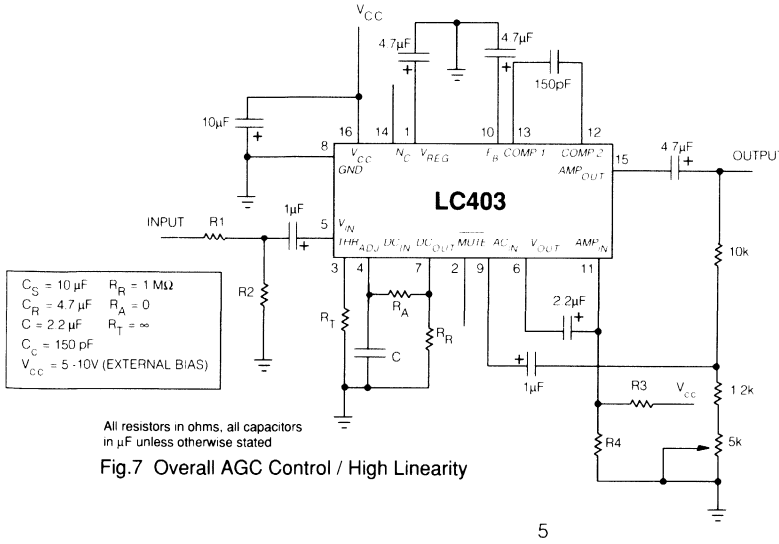


Fig.7 Overall AGC Control / High Linearity

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

AVAILABLE PACKAGING
16 pin DIP plastic or ceramic

SPD 1

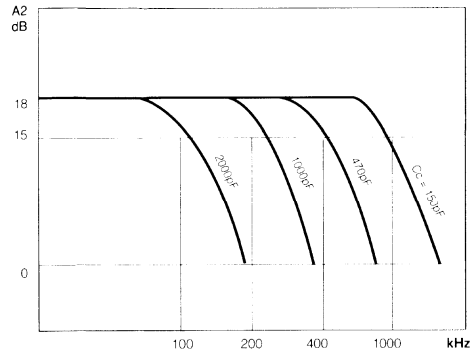


Fig.8 Amplifier Gain vs Frequency

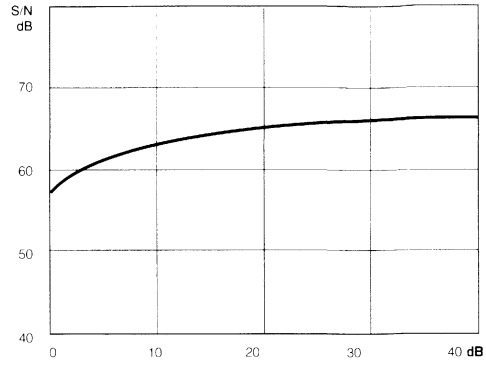


Fig.9 Output Signal to Noise vs Attenuation

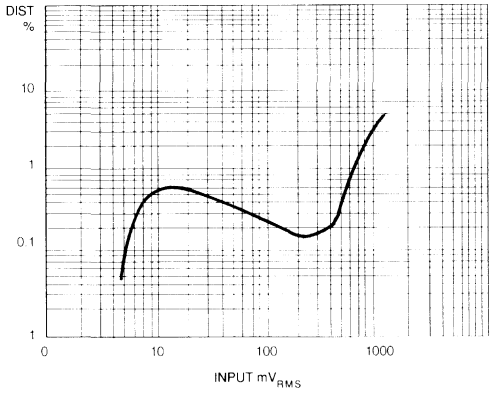
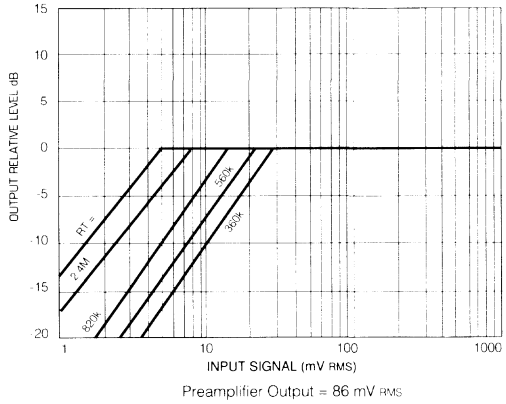


Fig.10 Distortion Function of Input Level
(AGC Mode) ($R_T = \infty$)



Preamplifier Output = 86 mV RMS
Amplifier Output = 680 mV RMS
t = 27°C

Fig. 11 AGC Characteristic

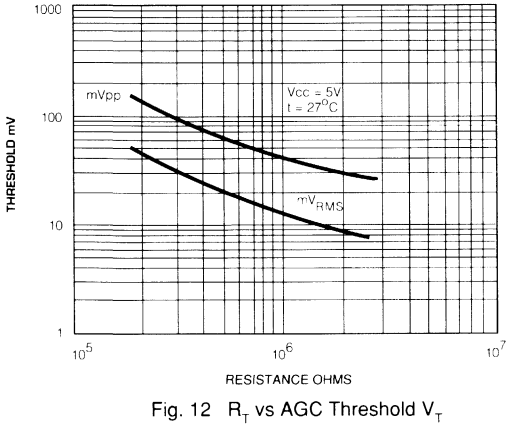


Fig. 12 R_T vs AGC Threshold V_T

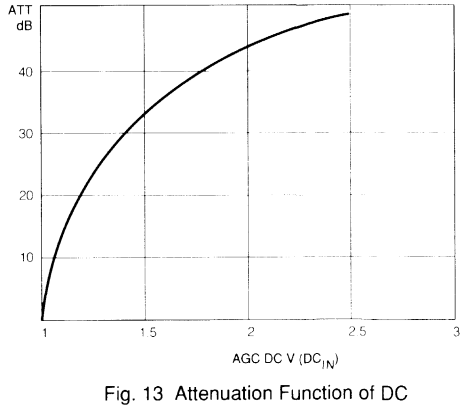


Fig. 13 Attenuation Function of DC Control Voltage

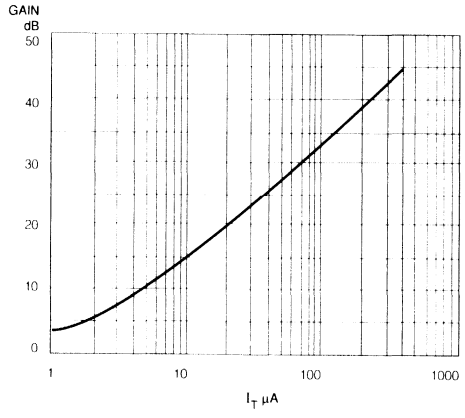


Fig.14 Attenuation vs Threshold Current I_T

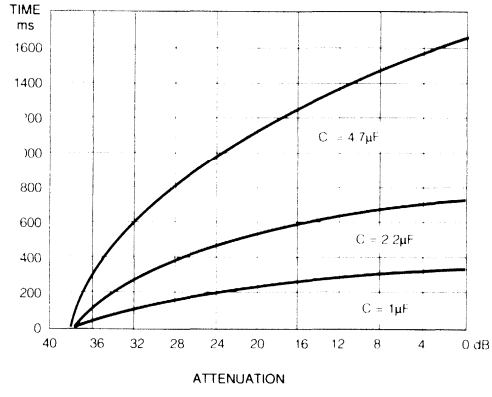


Fig.15 Release Time Characteristics
$R_R = 1M\Omega$ ($R_T = \infty$)

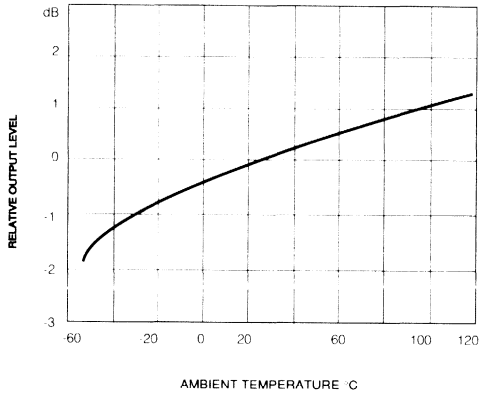


Fig. 16 Typical Output Level Function of Temperature (AGC Mode)

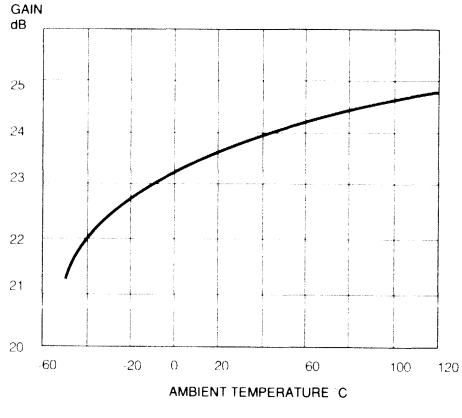
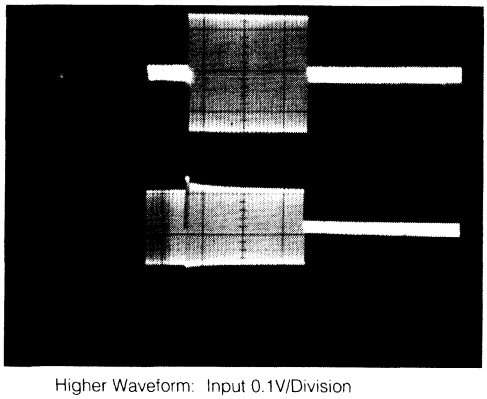
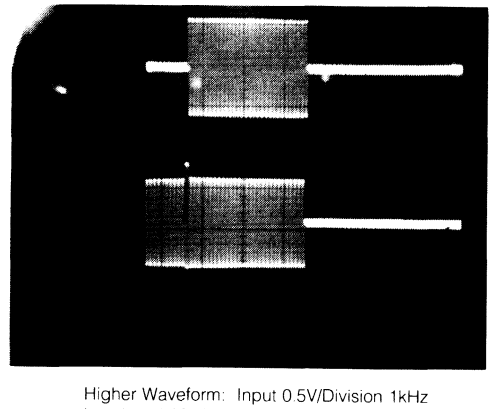


Fig.17 Typical Preamplifier Gain in Linear Mode (Attenuator Included)



Higher Waveform: Input 0.1V/Division
Low Level 30mVpp
High Level 300mVpp
Lower Waveform: Output 1V/Division

Fig. 18 Transient Characteristic



Higher Waveform: Input 0.5V/Division 1kHz
Low Level 60mVpp
High Level 1.2Vpp
Lower Waveform: Output 1V/Division

Fig. 19 Transient Characteristic

Low Voltage - Low Power Operational Amplifier LC810

PRELIMINARY DATA SHEET

FEATURES

- low voltage design - operates down to1.0 V total supply voltage
- low power consumption - 200 μA typical quiescent supply current
- single or dual supply operation
- class AB output stage swings virtually rail-to-rail

DESCRIPTION

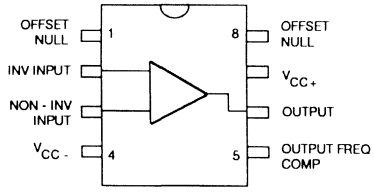
The LC810 is a silicon monolithic operational amplifier employing specialized circuit design techniques to enable operation on supply voltages as low as 1.0 V. The class AB output stage is designed to swing to within a single transistor saturation voltage of either supply rail, and can drive load impedance as low as 180 Ω. The PNP input stage has acommon mode input range which extends below the negative supply rail, making the amplifier ideal for single supply applications.

ABSOLUTE MAXIMUM RATING

Parameter	Value / Units
Power supply	6V
Differential input voltage	± 20
Input voltage range (either input; ref (Vcc-))	-0.7 to + 20V
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10s)	300°C

Pin Out

Top View



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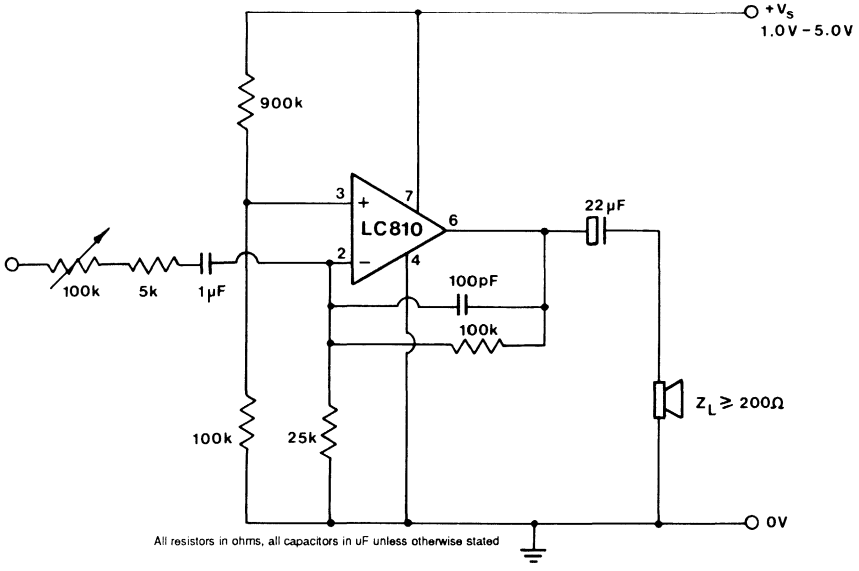

FUNCTIONAL DIAGRAM

Document No. 510 - 10 - 1

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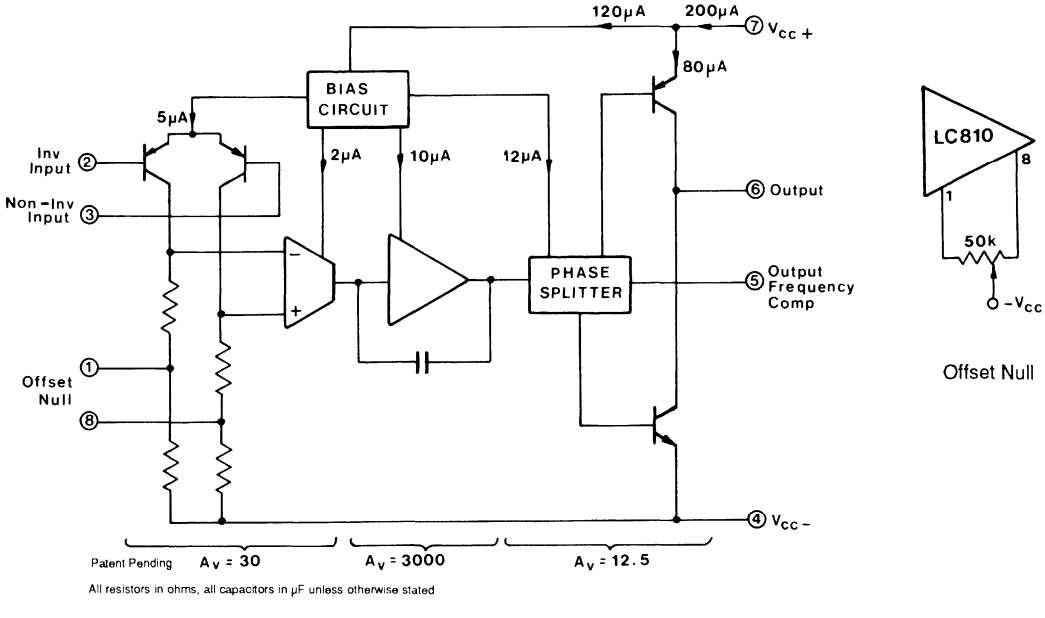
TYPICAL ELECTRICAL SPECIFICATIONS

Conditions: Ta = 25°C, Vs = (Vcc+) - (Vcc-) = 1.3V unless otherwise noted:

Parameter	Typical Value (Range)	Units
D.C. Voltage Gain	1000	V/mV
Input Resistance	1.0	MΩ
Input Offset Voltage	(±2.5)	mV
Input Bias Current	50	nA
Input Offset Current	(± 5)	nA
Gain-Bandwidth Product	600	kHz
Slew Rate	0.2	V/μs
Output Current	±5	mA
Output Current, Vs = 5V	+10, -50	mA
Output Current, Vs = 1.7V	+7, -30	mA
Max. Differential Input Signal	±20	V
Max. Common Mode Input Signal	(Vcc-)-0.3 to (Vcc+) -0.7)	V
Common Mode Rejection	110	dB
Power Supply Rejection	115	dB
Supply Current (no load, no signal)	200	μA



Typical LC810 Application Headphone Amplifier 0 - 26dB

SEMICUSTOM ARRAY PRODUCTS

SCD

data sheets

Gennum engineers and others
in our Marketing Department
are always available to discuss
any proprietary design/semicustom product
requirements you may have.
Please ask for our brochure BR508

SEMICUSTOM LINEAR ARRAYS DATA SHEET

ADVANTAGES OF THE SEMICUSTOM ARE:

- **custom circuitry at low cost**
- **quick turnaround**
- **high reliability**
- **design proprietorship**
- **reduced PCB size**

For complete information about Gennum linear array products, please refer to our Semicustom Design Manual. Kits and manuals are available from Gennum or your local representative.

CIRCUIT DESCRIPTION

The Gennum semicustom integrated circuits are arrays of bipolar transistors, p diffused resistors, pinch resistors, junction capacitors and Schottky diodes. The individual components on the chip are uncommitted.

The user can design his own proprietary circuit using the transistors, resistors, and capacitors available on the chip. Once the circuit is designed and tested with discrete components (provided with the design manual), the interconnection layout is generated and used to manufacture the proprietary circuit.

SEMICUSTOM BIPOLAR ARRAY COMPONENT LIST (20 V MAX. OPERATING VOLTAGE)

		LA250			LA200		
ACTIVE COMPONENTS		L A251	LA252	LA253	LA201	LA202	LA204
Small NPN	- standard	122	92	52	83	46	17
	- Schottky clamped	18	12	8	-	-	8
	- low noise	8	8	8	-	-	-
	Total	148	112	68	83	46	25
Large NPN	-ic ≤ 100mA	-	-	2	2	2	2
	- Ic ≤ 300mA	4	4	-	-	-	-
	Total	4	4	2	2	2	2
Lateral PNP	-split collectors (2)	36	24	16	26	14	9
	-multiple collectors (6)	13	10	4	-	-	-
	Total	49	34	20	26	14	9
Zener Diode		4	4	4	1	1	1
Large Diode		2	2	2	-	-	-
PASSIVE COMPONENTS							
Junction Capacitor	- 75 pF capacitors	4	4	4	3	3	-
	- 56 pF capacitors	-	-	-	-	-	3
	Total	4	4	4	3	3	3
Various P-Diffused Resistors (total resistance)		1000 K	670 K	340 K	450 K	240 K	170 K
40 K Pinch Resistors		28	28	20	10	8	6
BONDING PADS		40	32	24	24	18	14
CHIP SIZE (mils)		150 x 144	151 x 111	92 x 111	127 x 94	78 x 94	56 x 91

SCD 1

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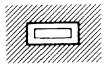
ULA COMPONENT DESCRIPTION

Legend for component drawings


Metallization


Contact


Emitter

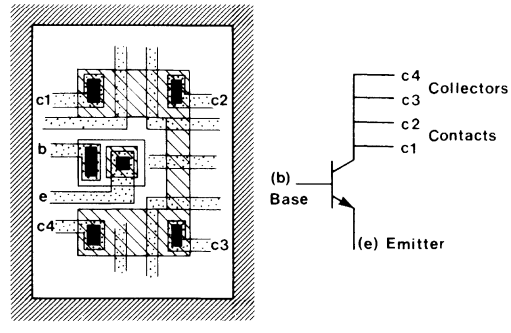

Base and Isolation


Base and Isolation in Zener Structure


DeepCollector Diffusion

Small Emitter NPN

The most common circuit element in the array and the one around which the process is optimized is the small npn cell. Since it is the most common cell, it makes sense to include the basic structure to implement cross-unders right in the layout. This is accomplished by making use of the low resistance emitter diffusion which forms the wrap-around collector structure, so that connections made to an npn collector on the circuit schematic may be made to any of the 4 collector contacts. It is not necessary for a particular npn to be used in the circuit before it can be used to implement a cross-under, in which case the transistor collector behaves like a low value resistor. In this mode, the base and emitter contacts should be shorted together.

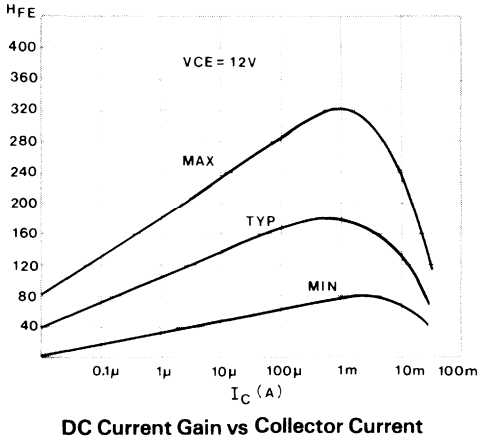


Small NPN Characteristics

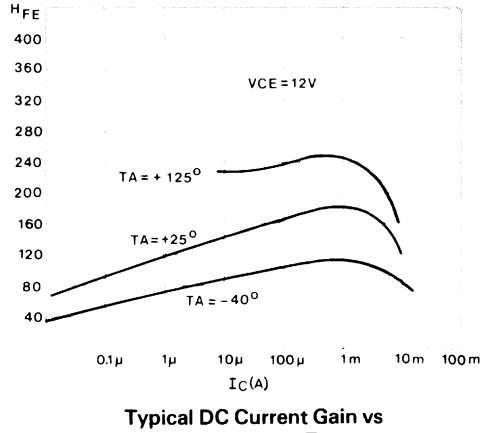
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA		270	400	mV
	I_C = 1 mA, I_B = .1 mA		100	200	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		10		pA
I_{CBO}	V_{CB} = 12 V		5		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.5		pF
f_T	I_C = 3 mA, V_{CE} = 12 V		250		MHz

ΔV_{BE} for adjacent devices 2mV typ (5mV max)

NPN Graphs

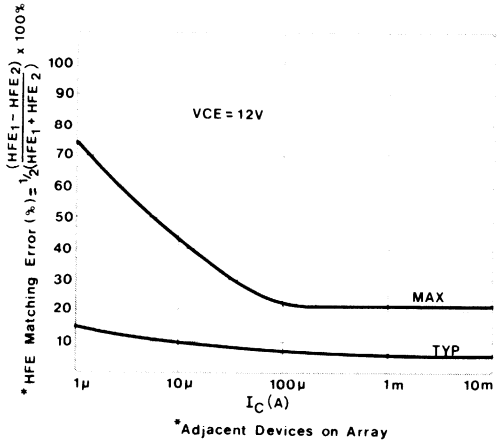


DC Current Gain vs Collector Current



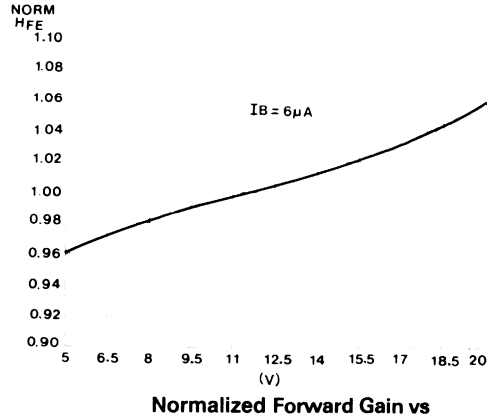
Typical DC Current Gain vs Collector Current over Temperature

NPN Graphs (continued)

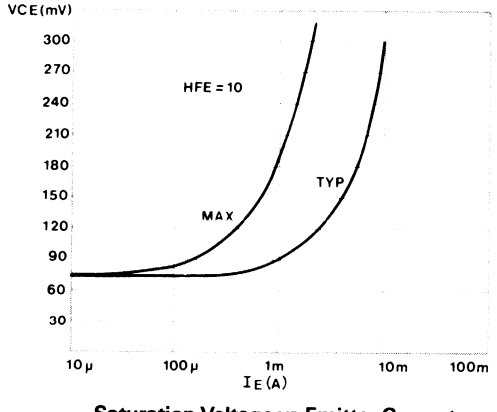


*Adjacent Devices on Array

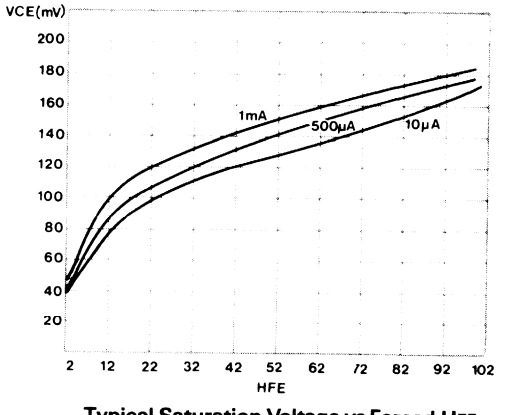
H_{FE} Matching Error (%)



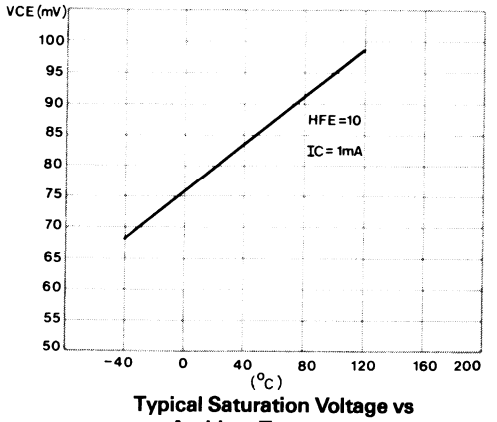
Normalized Forward Gain vs Collector Voltage



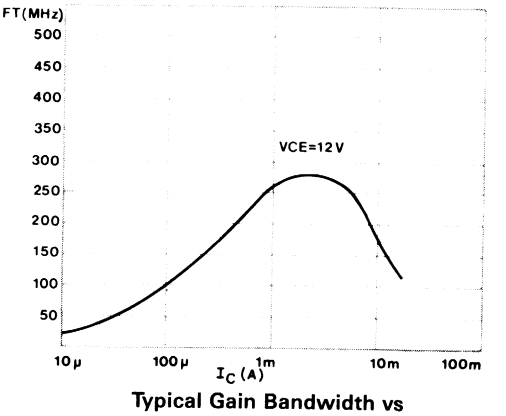
Saturation Voltage vs Emitter Current



Typical Saturation Voltage vs Forced H_{FE}

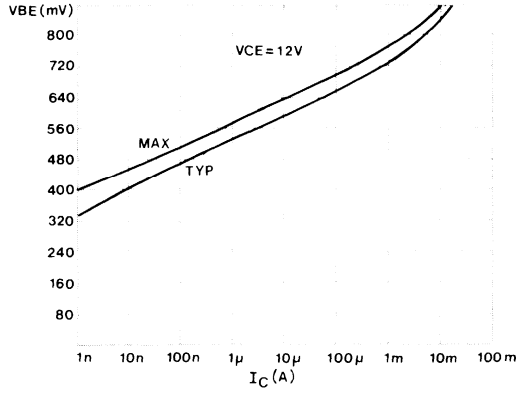


Typical Saturation Voltage vs Ambient Temperature

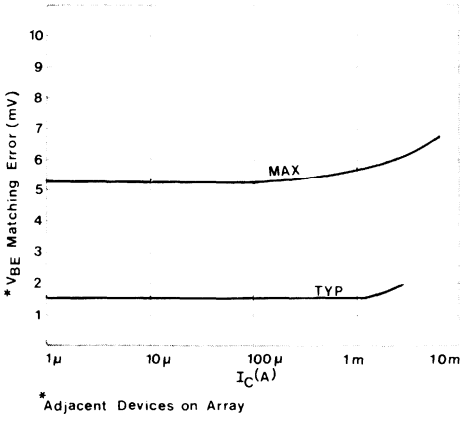


Typical Gain Bandwidth vs Collector Current

SCD 1



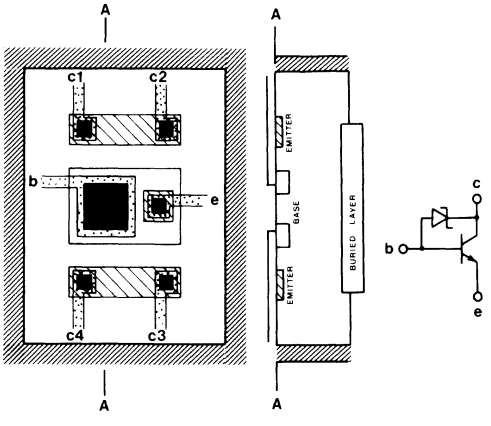
Base Emitter Voltage vs Collector Current



V_{BE} Matching Error

SCHOTTKY CLAMPED NPN

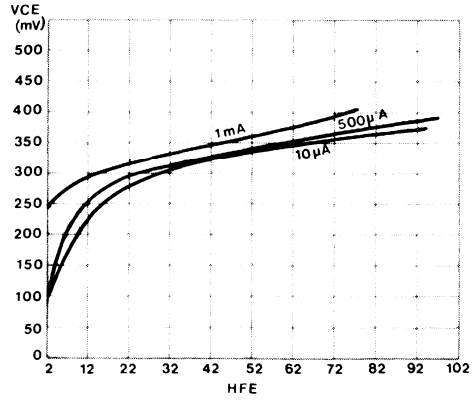
This npn transistor has an additional Schottky diode connected between its base and collector by allowingthe metal to contact the epitaxial layer through a hole in the base diffusion. This Schottky diode can prevent hard saturation when the cell is used as an npn transistor, or it may be accessed independently with the base and collector contacts. Since this transistor cell is not suitable in low saturation applications, the normal wrap-around collector has been replaced by two separate pick-ups which may still be used as low resistance cross-unders, with the resistance between the two collector pick-ups as approximately 150 Ω.



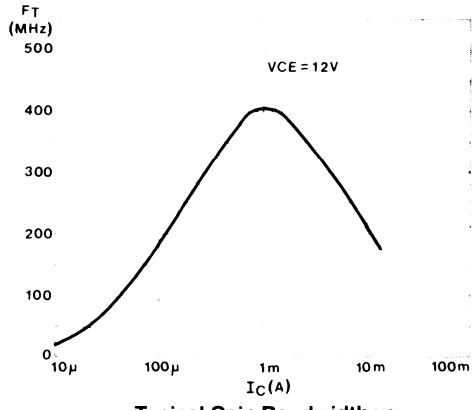
Schottky NPN Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
V_{BC}	I_C = -10 μA, I_B = 10 μA		410	450	mV
$V_{CE(SAT)}$	I_C = 10 μA, I_B = 1 μA	200	290		mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		200		pA
I_{CBO}	V_{CB} = 12 V		20		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.7		pF
f_T	I_C = 1 mA, V_{CE} = 12 V		400		MHz

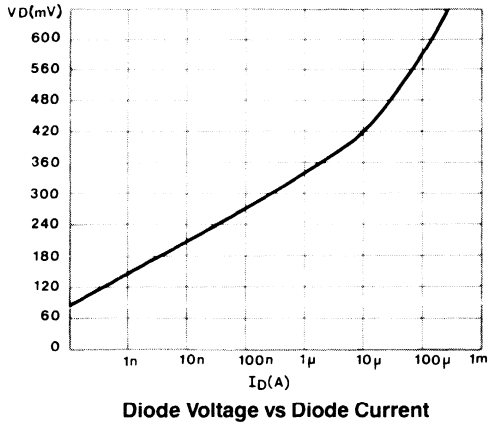
Schottky Graphs



Typical Saturation Voltage vs Forced HFE



Typical Gain Bandwidth vs Collector Current

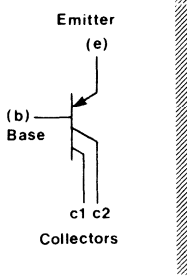


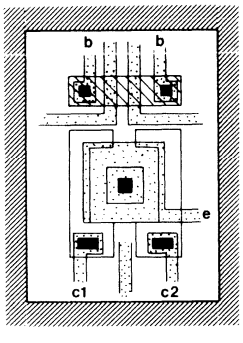
Diode Voltage vs Diode Current

Note: For characteristics not shown see section on Small Emitter NPN

SPLIT COLLECTOR PNP

The pnp transistors are of the lateral action construction with the collector split into two equal segments.
This structure may be used as a single pnp when both collectors are connected together. It may also be considered as two pnp transistors with common emitters and common bases. When considered as two transistors it can be used to implement current sources, current mirrors and area ratios on an integrated circuit.





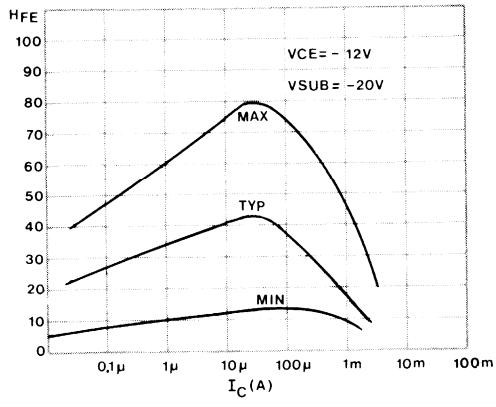
SCD 1

Split Collector PNP (with both collectors connected together)

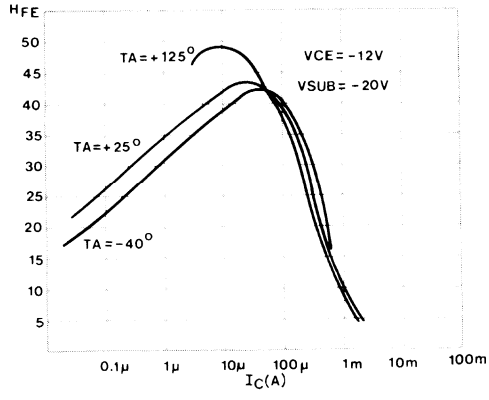
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 30 µA, V_{CE} = -12 V, V_{SUB} = -20 V	15	40		
V_{BE}	I_C = 10 µA, V_{CE} = -12 V, V_{SUB} = -20 V	540	600		mV
$V_{CE(SAT)}$	I_C = 100 µA, I_B = 50 µA, V_{SUB} = -20 V		90	120	mV
BV_{CEO}	I_C = 20 µA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 µA, I_C = 0	20	27		V
I_{CEO}	V_{CE} = -12 V		100		pA
I_{CBO}	V_{CB} = -12 V		5		pA
V_A	I_B = 10 µA, V_{CE} = -5 V and -15 V	30	42		V
C_{OB}	f = 1 kHz, V_{CB} = 0		0.96		pF
f_T	I_C = 100 µA, V_{CE} = -12 V, V_{SUB} = -20 V		3.5		MHz

ΔV_{BE} for adjacent devices 2mV typ (6mV max)

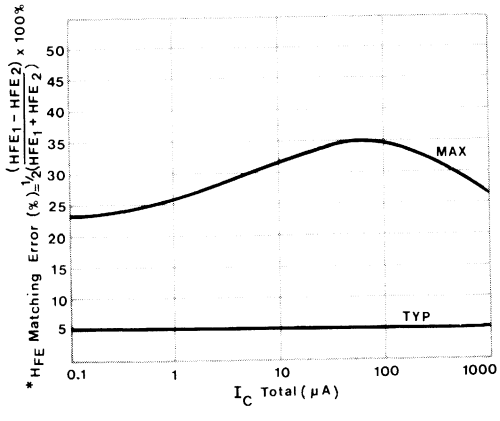
PNP Graphs



DC Current Gain vs Collector Current

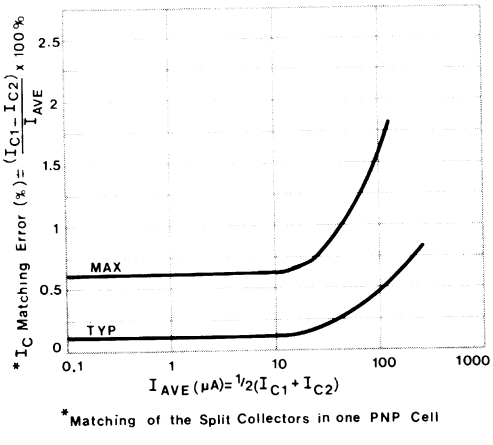


Typical DC Current Gain vs Collector Current over Temperature



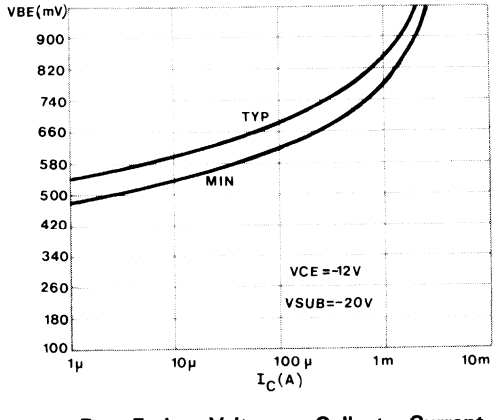
*Adjacent Devices on Array with both Collectors joined

H_{FE} Matching Error

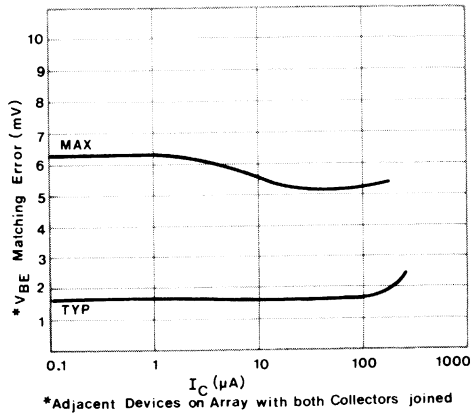


*Matching of the Split Collectors in one PNP Cell

Collector Current Matching (%)



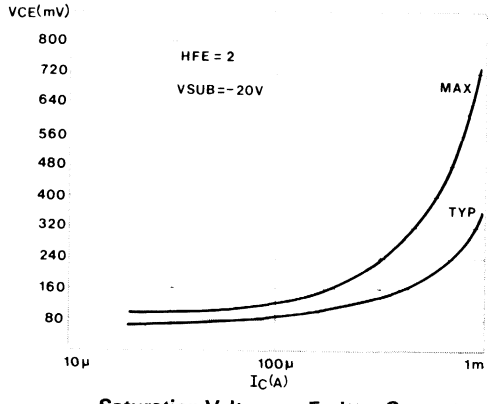
Base Emitter Voltage vs Collector Current



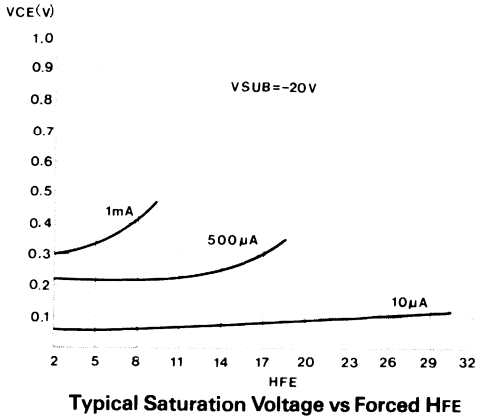
*Adjacent Devices on Array with both Collectors joined

V_{BE} Matching Error

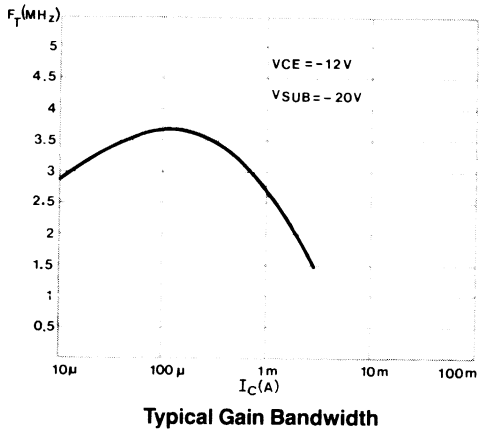
PNP Graphs (continued)



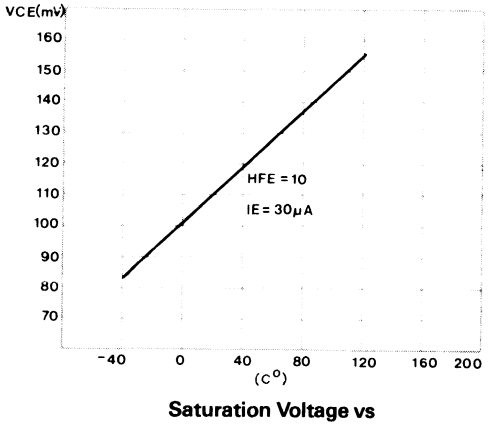
Saturation Voltage vs Emitter Current



Typical Saturation Voltage vs Forced HFE



Typical Gain Bandwidth vs Collector Current



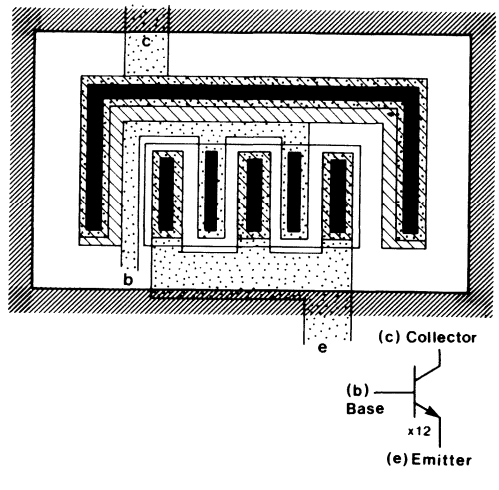
Saturation Voltage vs Ambient Temperature

SCD 1

LARGE NPN

This is approximately equivalent to 12 small npns connected in parallel. Since there are only two in the array, no provision has been made for cross-unders in this structure, although care has been taken to allow the base connection to be made from either side of the transistor. Note that each of these transistors can pass substantial current but the main limiting factor is probably the power being dissipated by the device. Here, the power is the product of the voltage across the transistor and the current in the collector, e.g. $P_d = V_{CE} \cdot I_C$.

This is one contribution to the overall power being dissipated on the die, which should be limited according to the chosen package.

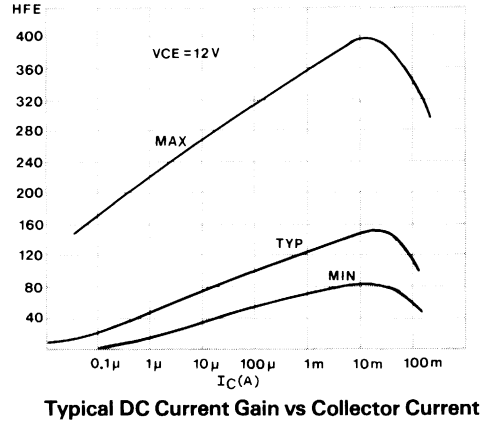


Large NPN Characteristics

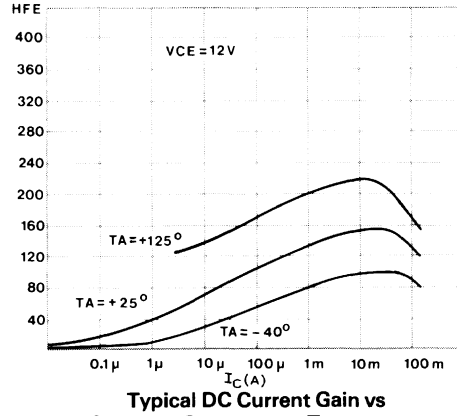
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 12 mA, V_{CE} = 12 V	80		400	
V_{BE}	I_C = 10 mA, V_{CE} = 12 V		790	850	mV
	I_C = 1 mA, V_{CE} = 12 V		680	740	mV
$V_{CE(SAT)}$	I_C = 1 mA, I_B = 1 mA		60	100	mV
	I_C = 10 mA, I_B = 1 mA		160	350	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		15		pA
I_{CBO}	V_{CB} = 12 V		30		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		10.7		pF
f_T	I_C = 18 mA, V_{CE} = 12 V		350		MHz

1mV typ (5mV max)

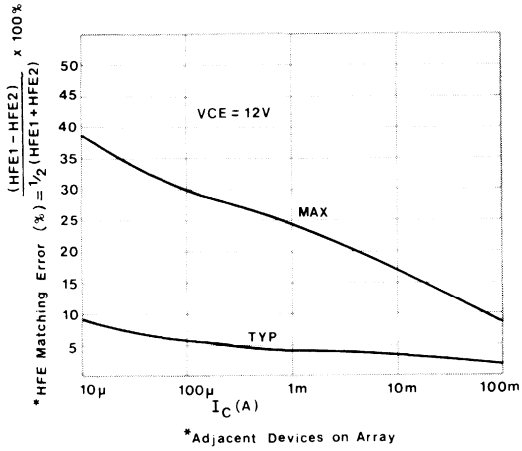
Large NPN Graphs



Typical DC Current Gain vs Collector Current

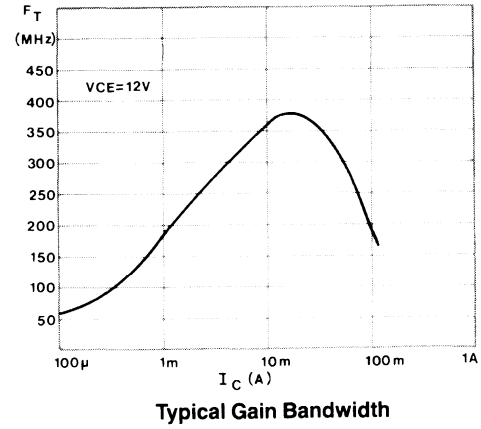


Typical DC Current Gain vs Collector Current over Temperature



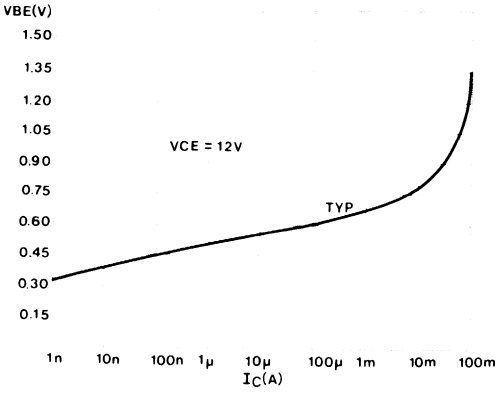
*Adjacent Devices on Array

H_{FE} Matching Error

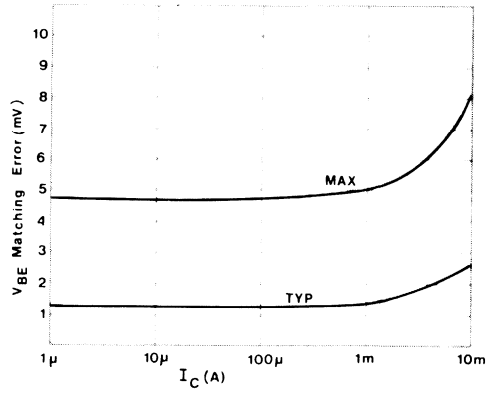


Typical Gain Bandwidth vs Collector Current

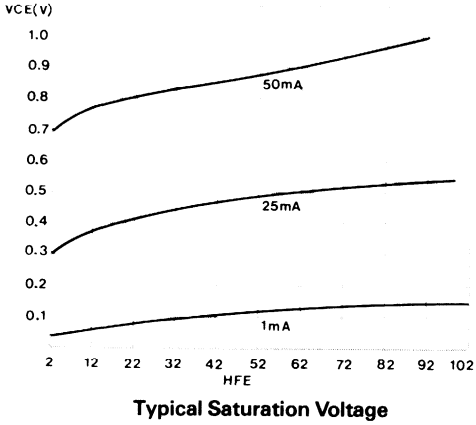
Large PNP Graphs



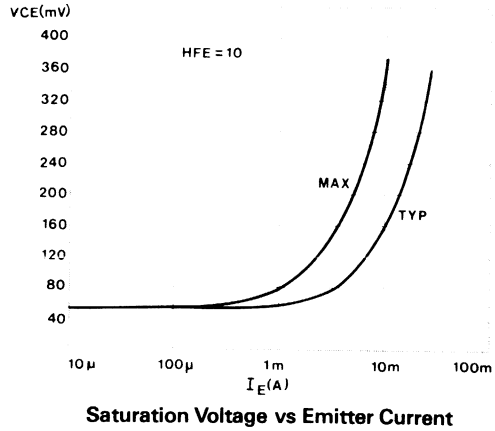
Base Emitter Voltage vs Collector Current



V_{BE} Matching Error

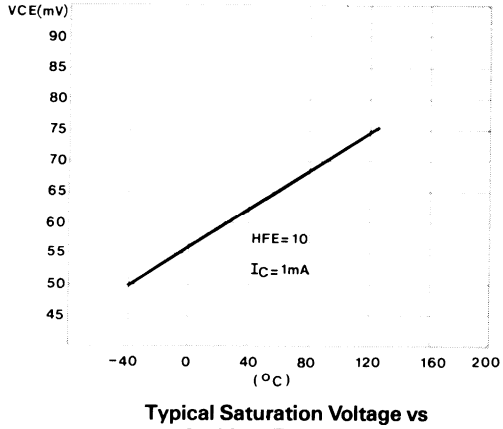


Typical Saturation Voltage vs Forced HFE



Saturation Voltage vs Emitter Current

SCD 1



Typical Saturation Voltage vs Ambient Temperature

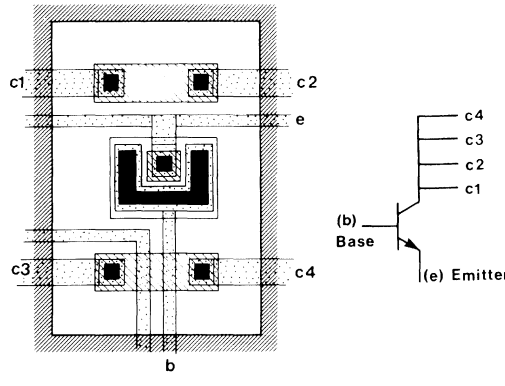
LOW NOISE NPN

Legend for component drawings

Metallization | Contact | Emitter | Base and Isolation | Base on Isolation in Zener Structure | Deep Collector Diffusion

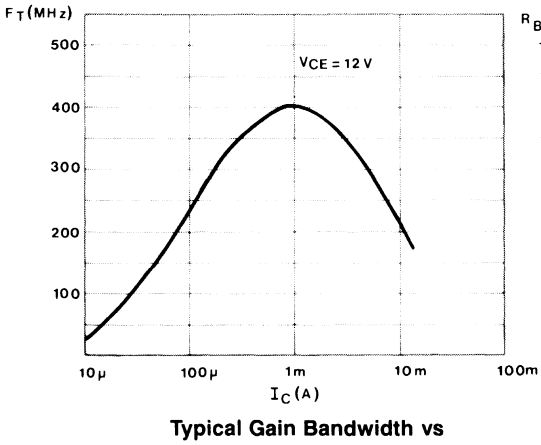
This device features a large base contact area which provides lower noise and better high frequency performance than the standard small npn.

Although intended primarily for the input stages of amplifiers, it may also be used for any standard small npn applications. The two collector pick-ups may be used as cross-unders if required, and in this respect the device is similar to the Schottky npn transistor.

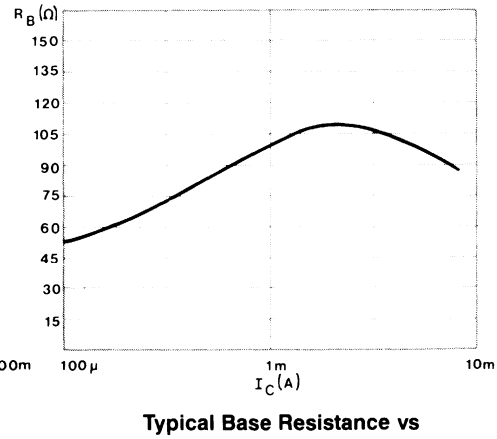


Low Noise NPN Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA		270	400	mV
	I_C = 1 mA, I_B = 1 mA		100	200	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		12		pA
I_{CBO}	V_{CB} = 12 V		6		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.7		pF
f_T	I_C = 3 mA, V_{CE} = 12 V		350		MHz

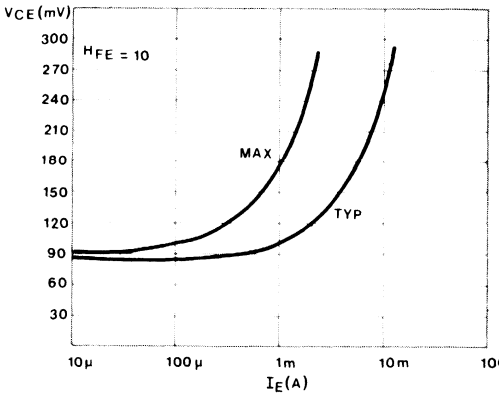


Typical Gain Bandwidth vs Collector Current

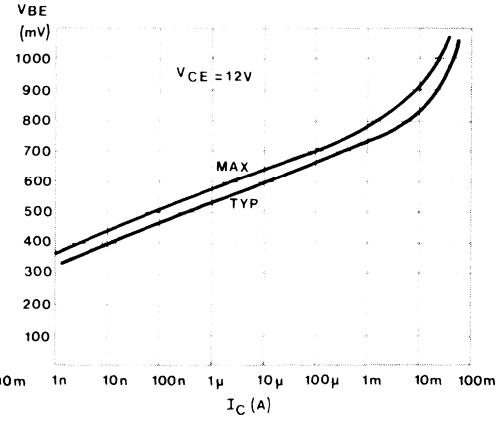


Typical Base Resistance vs Collector Current

Low Noise NPN Graphs (continued)



Saturation Voltage vs Emitter Current



Base Emitter Voltage vs Collector Current

Note: For characteristics not shown see section on Small Emitter NPN

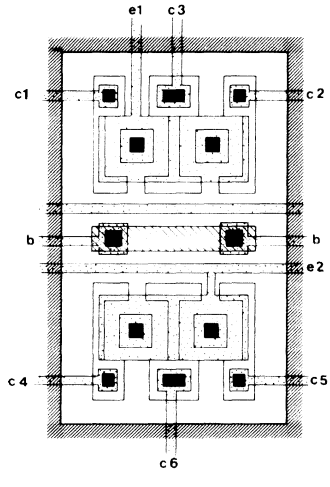
MULTIPLE COLLECTOR PNP

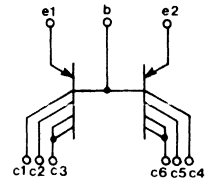
These pnp transistors are of the lateral action construction with the collector split in six segments.

Collectors c1, c2, c4 and c5 have the same effective "emitter area" as standard split collector pnp's. Collectors c3 and c6 are "double area".

The device can be used as a multiple current source or by connecting all collectors together as a pnp with better current handling, i.e. peak H_{FE} approx .- 120 µA.

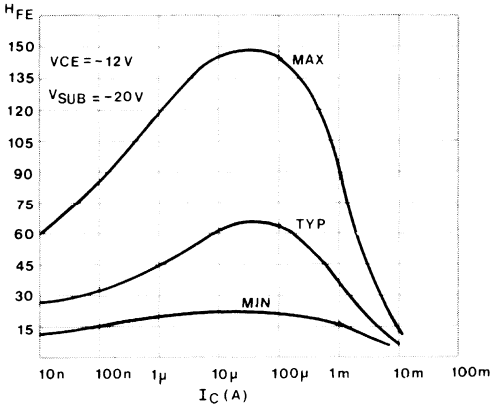
We suggest e1 and e2 be shorted together to prevent possible crosstalk between emitters. If c6 and c3 are considered as two single collectors in parallel, then the current matching performance of the collectors is as described by the collector current matching graph for the twin collector PNP.



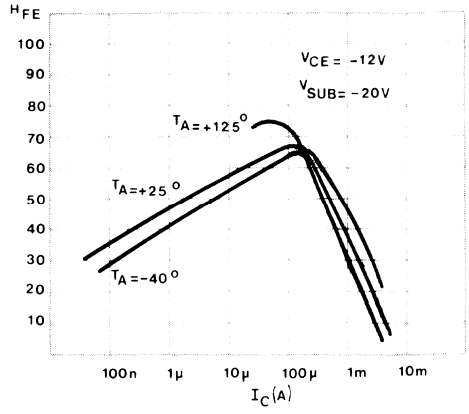


SCD 1

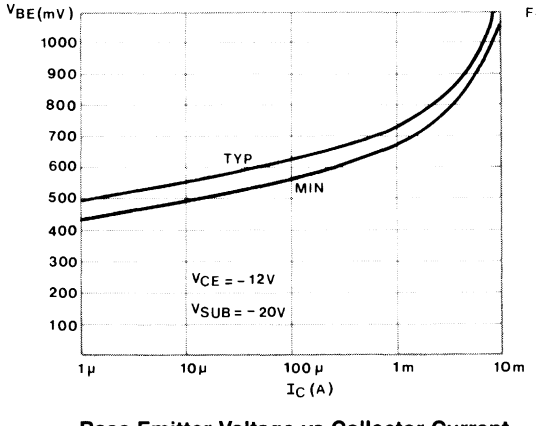
Multiple Collector PNP (with all collectors connected together and emitters connected together)					
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 120 µA, V_{CE} = −12 V, V_{SUB} = −20 V	20	65		
V_{BE}	I_C = 40 µA, V_{CE} = −12 V, V_{SUB} = −20V	540	600		mV
$V_{CE(SAT)}$	I_C = 400 µA, I_B = 200 µA, V_{SUB} = −20 V		90	120	mV
BV_{CEO}	I_C = 20 µA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 µA, I_C = 0	20	27		V
I_{CEO}	V_{CE} = −12 V		400		pA
I_{CBO}	V_{CB} = −12 V		20		pA
V_A	I_B = 10 µA, V_{CE} = −5 V and −15 V	30	70		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.8		pF
f_T	I_C = 400 µA, V_{CE} = −12 V, V_{SUB} = −20 V		3.5		MHz



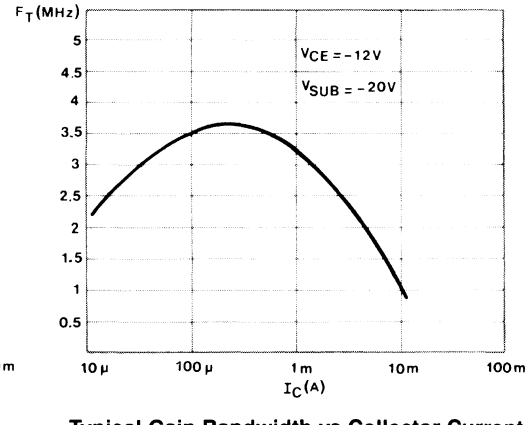
DC Current Gain vs Collector Current



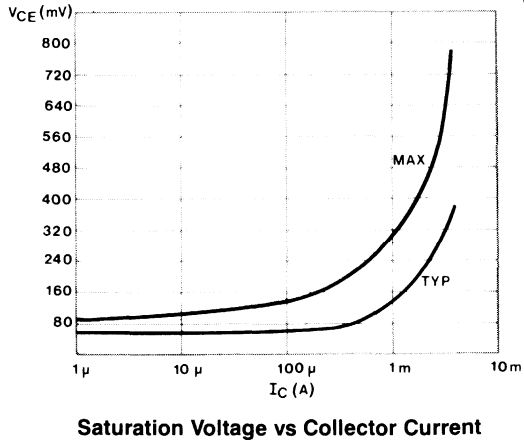
Typical DC Current Gain vs Collector Current over Temperature



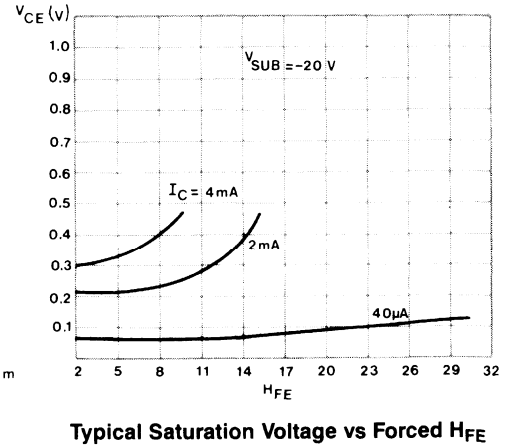
Base Emitter Voltage vs Collector Current



Typical Gain Bandwidth vs Collector Current

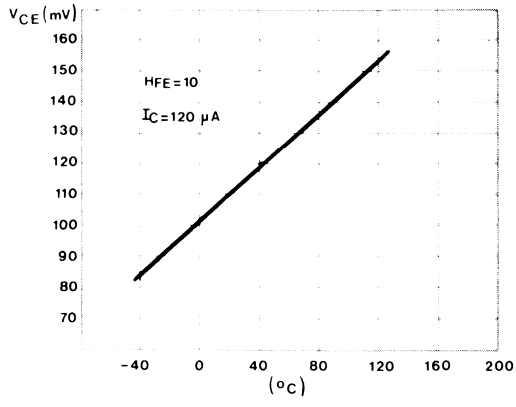


Saturation Voltage vs Collector Current



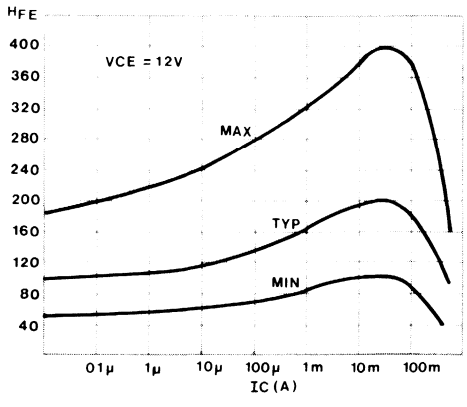
Typical Saturation Voltage vs Forced H_{FE}

Multiple Collector PNP Graphs (continued)



Typical Saturation Voltage vs Ambient Temperature

Power NPN Graph



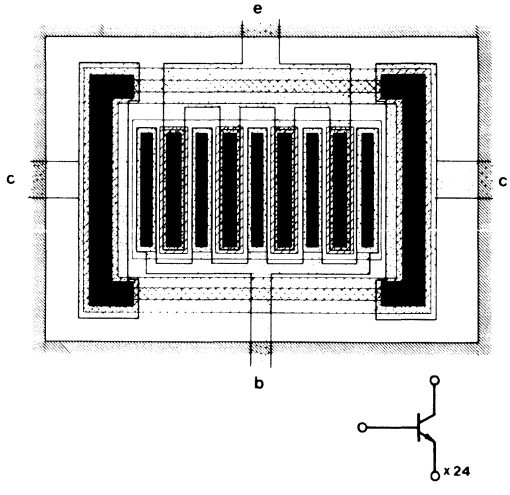
DC Current Gain vs Collector Current

POWER NPN

This transistor has approximately twice (2x) the emitter area of the large npn device on the LA200 series arrays and twenty four times (24x) the emitter area of the small npn; hence a correspondingly higher current capability (I_C max. = 300 mA). In addition to being physically larger, the device has a number of extra features which offer an enhanced performance over the LA200 series large npn.

These features are:

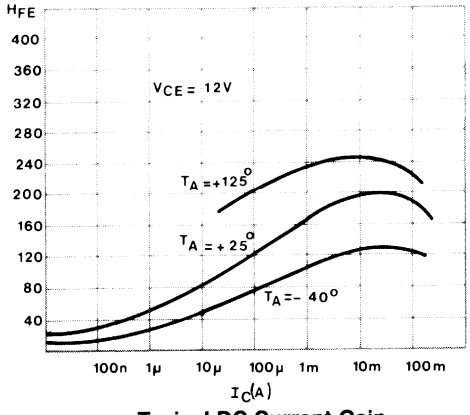
- Four separate emitter structures to provide improved gain at high collector currents.
- Five base contacts to reduce the VBE for high base currents and improve switching speed.
- An all-around deep collector diffusion to ensure a low saturation voltage in switching applications.



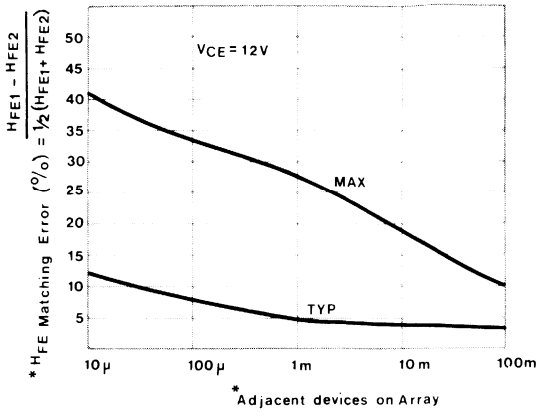
SCD 1

Power NPN Characteristics

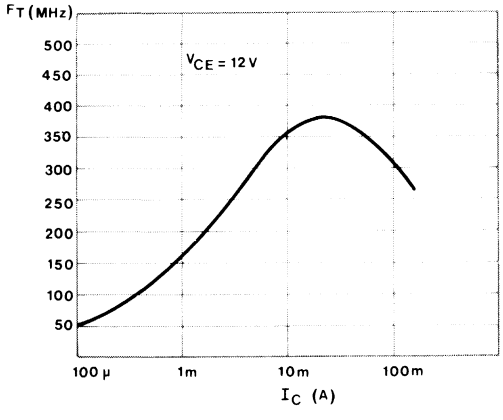
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 20 mA, V_{CE} = 12 V	100		400	
V_{BE}	I_C = 10 mA, V_{CE} = 12 V		660		mV
	I_C = 1 mA, V_{CE} = 12 V		595		mV
$V_{CE(SAT)}$	I_C = 1 mA, I_B = 1 mA		15	26	mV
	I_C = 10 mA, I_B = 1 mA		50	100	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		50		pA
I_{CBO}	V_{CB} = 12 V		25		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		14		pF
f_T	I_C = 36 mA, V_{CE} = 12 V		350		MHz



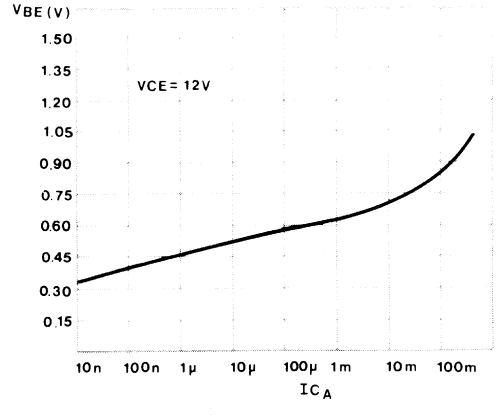
Typical DC Current Gain vs Collector Current over Temperature



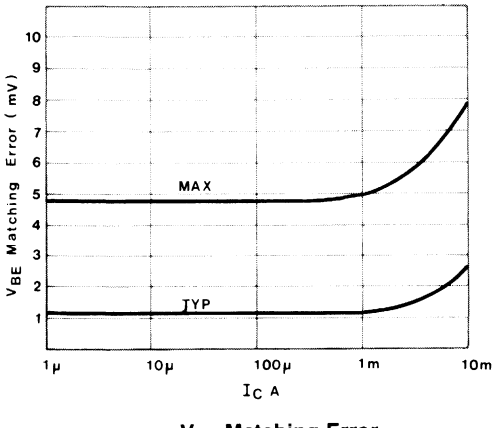
H_{FE} Matching Error



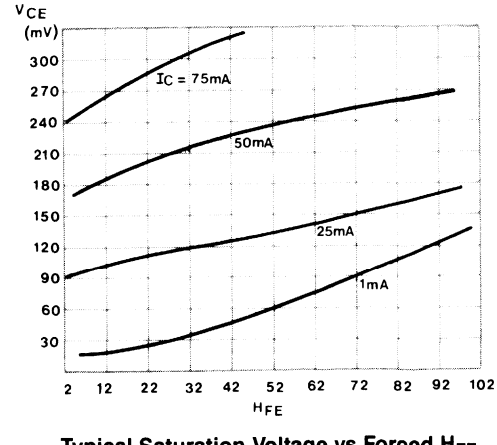
Typical Gain Bandwidth vs Collector Current



Typical Base Emitter Voltage vs Collector Current

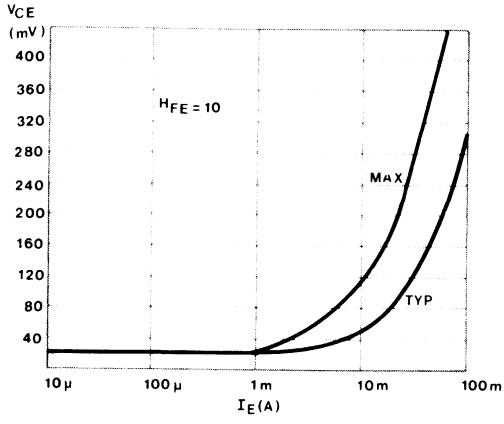


V_{BE} Matching Error



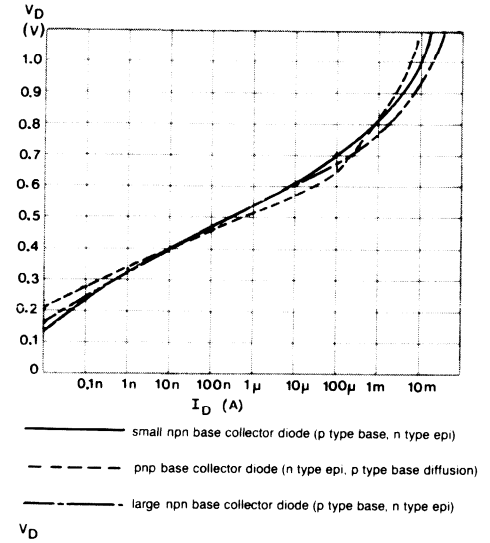
Typical Saturation Voltage vs Forced H_{FE}

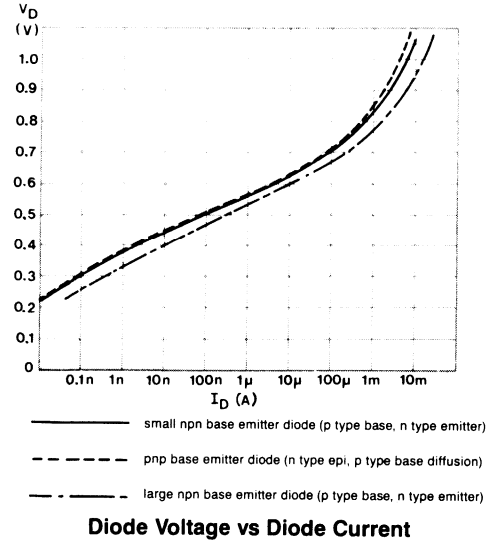
Power NPN Graph (continued)



Saturation Voltage vs Emitter Current

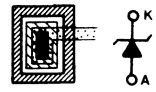
Zener Diode Graphs





Diode Voltage vs Diode Current

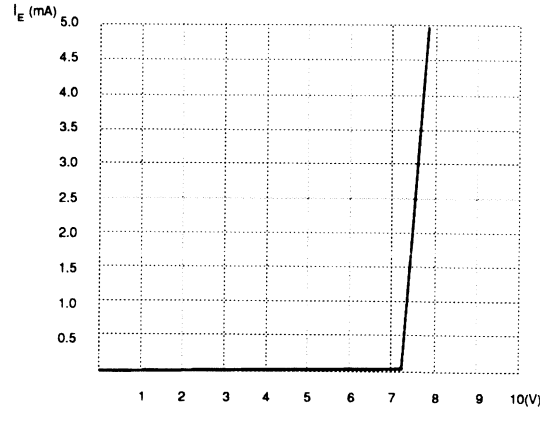
ZENER DIODE



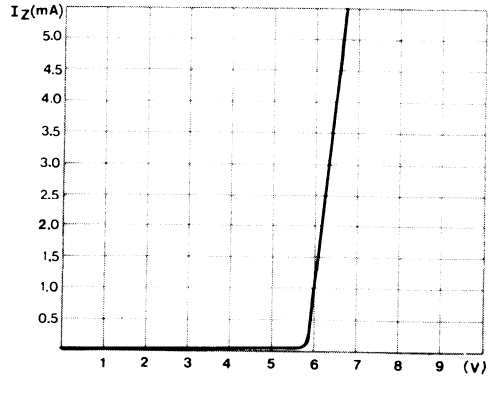
Anode to substrate

This is a generally accepted term for any p-n junction used in thereverse breakdown mode. The voltage at which the reverse biased junction starts to pass significant current is a function of the doping levels of the p-type and the n-type semi-conductor in question. Any number of components on the array may be used in such a way that it will break down a junction and pass current, however, the voltage at which this happens directly affects the temperature coefficient of the resulting reference voltage. The zener diode which is specifically provided as a voltage reference has a breakdown of approximately 5.8 V with respect to substrate. The sandwich capacitors may be used in this mode with a zener diode breakdown of approximately 5.8 V ±0.5 V across the capacitor contacts and without respect to substrate. The temperature coefficient of breakdown voltage is +200 ppm/°C.

Any npn transistor may be used as a zener reference by reverse biasing the base-emitter junction which will break down at approximately 7.5 V with a slope resistance of 100 Ω.



Breakdown Voltage of Reverse Biased Base – Emitter Junction of Small NPN



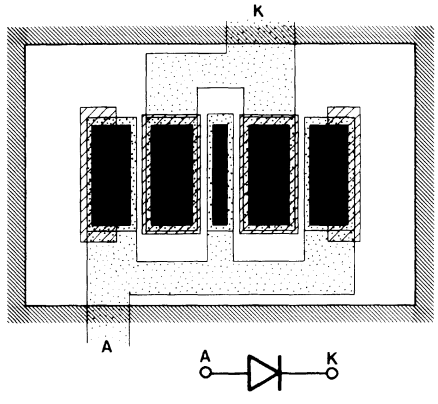
Zener Diode Breakdown Characteristics

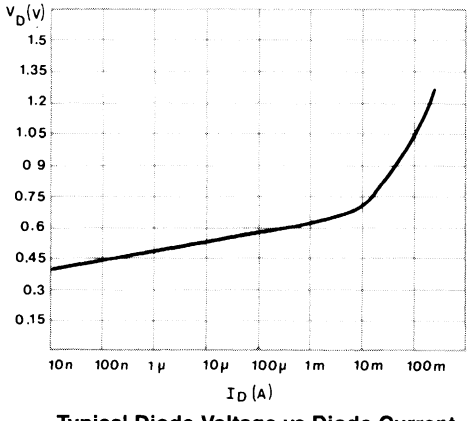
SCD 1

DIODES

Large Diode

Two large diodes are provided on the LA251 ans LA252 arrays for applications where high forward current is required. The reverse breakdown characteristic is similar to that of an npn base-emitter junction.





Typical Diode Voltage vs Diode Current

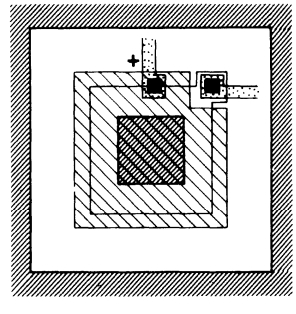
Implementing Diodes using Array Transistors

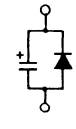
		Diode Voltage at 10 μA	Reverse Breakdown Voltage
Small/Low noise npn	base - emitter	0.6	7.5 V
Small/Low noise npn	base - collector	0.6	>20 V
Small/Multiple pnp	base - emitter	0.6	>20 V
Schottky npn	base - collector	0.4	>20 V
Large/Power npn	base - emitter	0.6	7.5 V
	base - collector	0.6	>20 V

CAPACITORS

The three large area capacitors which are in the corners of the die are junction capacitors with an emitter (diffusion) on base (diffusion) on isolation construction which is often referred to as a *sandwich capacitor*. This type of capacitor has an equivalent circuit as shown: Thus the forward bias voltage is approximately 0.6 V and the reverse bias breakdown voltage is that of the zener diode at 5.8 V (approximately). The nominal value is 75 pF.

In addition, the intrinsic capacitance of any of the structures may be used. In particular, the reverse biased collector to base junction of the npn structures may be used at any voltage up to 20 V.

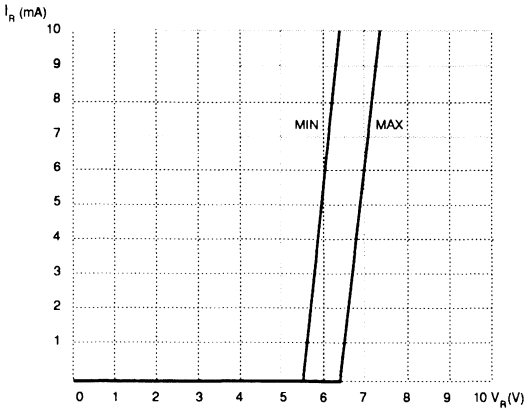




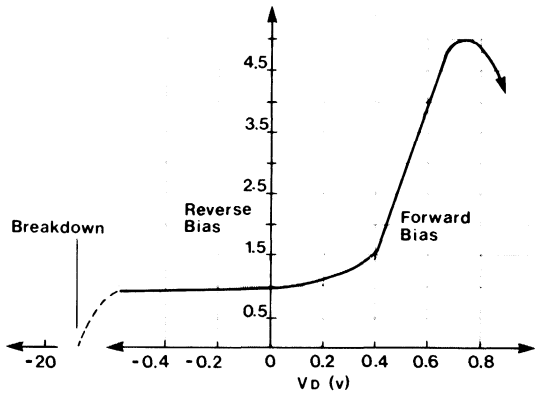
Capacitors

TYPE	NOMINAL VALUE	TOLERANCE OF NOMINAL	ZENER BREAKDOWN VOLTAGE	TEMPERATURE COEFFICIENT OF BREAKDOWN VOLTAGE
Sandwich	*75 pF	± 20%	5.8 V ± 0.5 V	+ 200 ppm/°C
Collector-Base Junction of small npn	0.4pF	± 20%	> 20 V	Do not use in breakdown mode
Collector-Base Junction of large npn	4.7 pF	± 20%	> 20 V	Do not use in breakdown mode
Emitter-Base Junction of small npn	0.7pF	± 20%	7.5 ± 1 V	+ 500 ppm/°C
Emitter-Base Junction of large npn	5.7 pF	± 20%	7.5 ± 1 V	+ 500 ppm/°C

* 56 pF on LA204 array



Reverse Breakdown Characteristic of Sandwich Capacitor

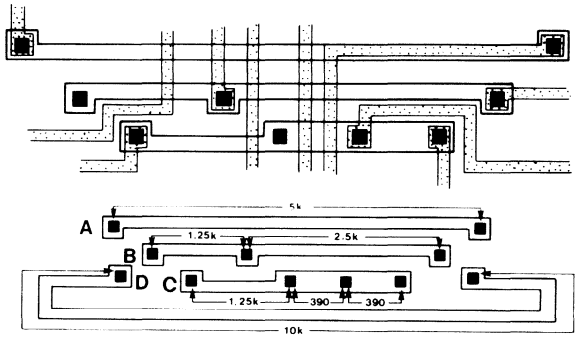


Normalized Capacitance (with respect to C_{JO}) for a PN Junction Capacitor

RESISTORS

All the resistors in the common land are formed during the base diffusion for the npn transistors and are termed "base resistors".

They have nominal values of 10 k (250 series only), 5 k, 2.5 k, 1.25 k and 390 Ω as shown on the diagram of a resistor grouping but their absolute values are dependent on the base diffusion sheet resistivity and so may have a variation of ±25%. However, a ratio of one resistor to another is considerably better and for identical resistors lying side by side on the die the matching tolerance will be ±4% at the three sigma points.



SCD 1

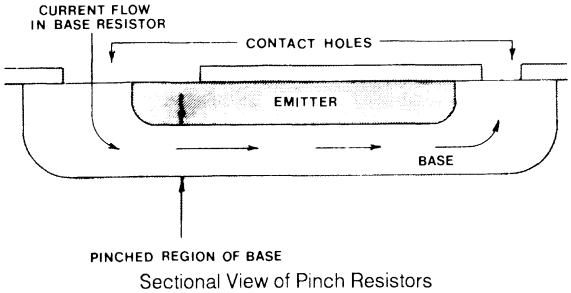
Notes
1 Resistor values are shown in ohms and are the resistance between adjacent contacts.
2 In the above combination of narrow and wide resistors matching is worse than for like types.

Resistors

TYPE	NOMINAL VALUE	ABSOLUTE TOLERANCE	MATCHING TOLERANCE	TEMPERATURE COEFFICIENT
A	5 k	± 25%	± 4%	+ 2000 ppm/°C
B	2.5 k	± 25%	± 4%	+ 2000 ppm/°C
	1.25 k			
C	1.25 k	± 25%		+ 2000 ppm/°C
	390		± 2%	
	390		± 2%	
D	10 k	± 25%	± 4%	+ 2000 ppm/°C
Pinch	40 k	+ 100% − 50%	± 15%	+ 5000 ppm/°C

PINCH RESISTORS

A pinch resistor is formed by putting emitter diffusion on top of a base resistor so that theeffective thickness of the resistor is greatly reduced. In this way, the resistance may be increased by a factor of ten.

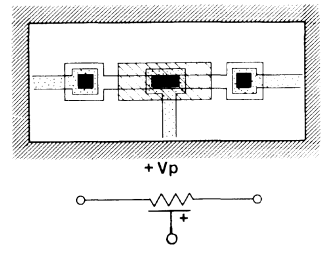


Sectional View of Pinch Resistors

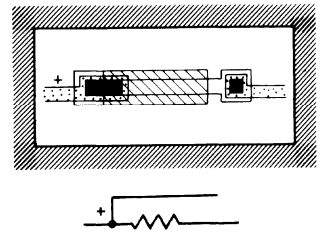
By applying a bias voltage to the emitter region, the associated depletion region further pinches off the base resistor until the reverse breakdown voltage is reached. Since this is the same as a reverse biased base emitter junction of an npn transistor, the pinch resistor will break down at approximately 7.5 volt. A full description of the voltage dependence of the resistor as the bias voltage is applied is shown on the graph Pinch Resistance vs Applied Voltage.

LA250 SERIES PINCH RESISTOR

This is essentially the same device as on the LA200 series, except a separate contact is provided for applying the bias voltage, allowing greater flexibility in layouts. As always, the bias contact should be connected to the most positive end of the resistor.



LA250 Small Series Pinch Resistor

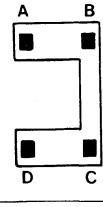


CROSS - UNDERS

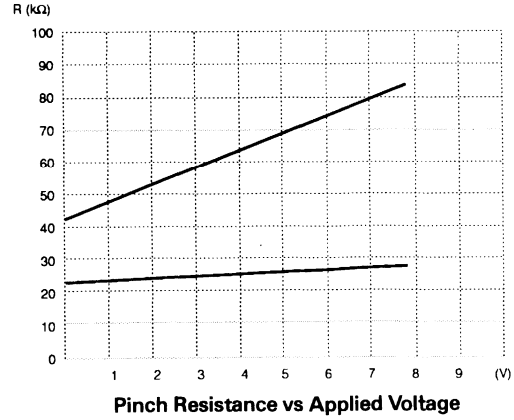
Standard Small NPN

The resistance between the four collector contacts is distributive, hence it is best described by a matrix.
e.g. R_{AC} = 20 Ω

Ω	B	C	D
A	7	20	23
B	-	16	20
C	16	-	7

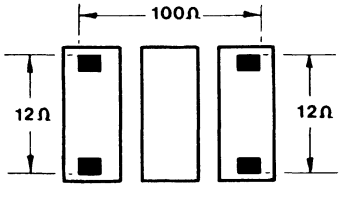


Additional Data for Emitter Diffusion Resistors (cross - unders)		
ABSOLUTE TOLERANCE	MATCHING TOLERANCE	TEMPERATURE COEFFICIENT
± 50%	± 5%	+ 600 ppm/°C

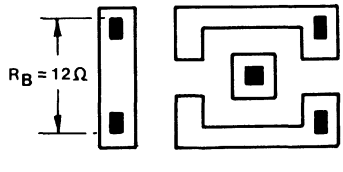


Pinch Resistance vs Applied Voltage

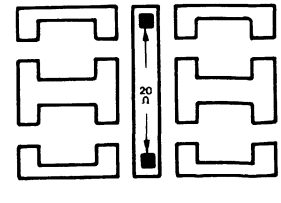
SCHOTTKY/LOW NOISE NPN

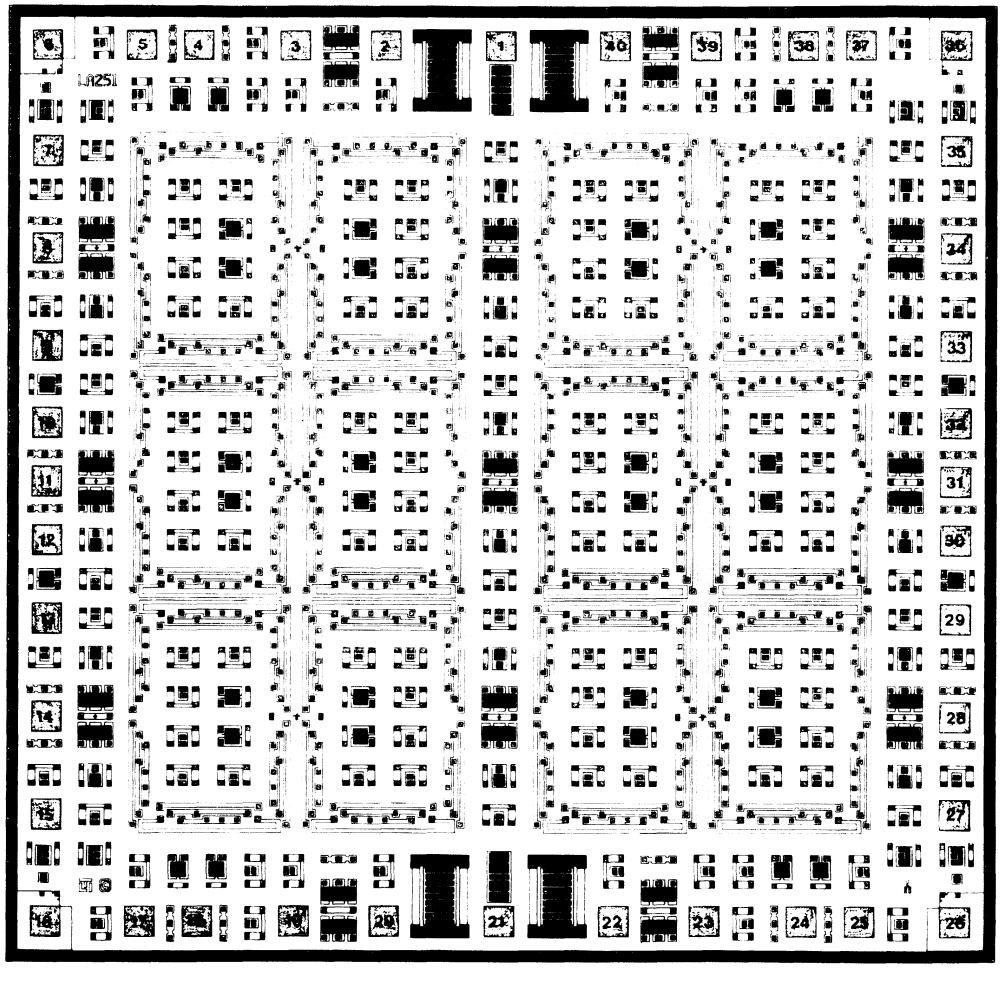


SPLIT COLLECTOR PNP BASE



MULTIPLE COLLECTOR PNP BASE

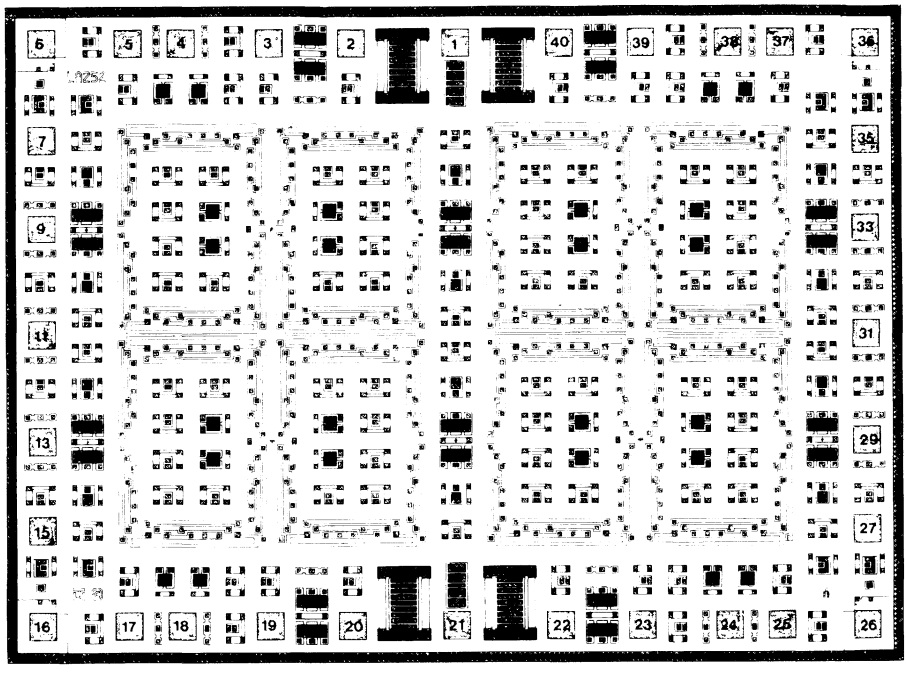




SCD
1

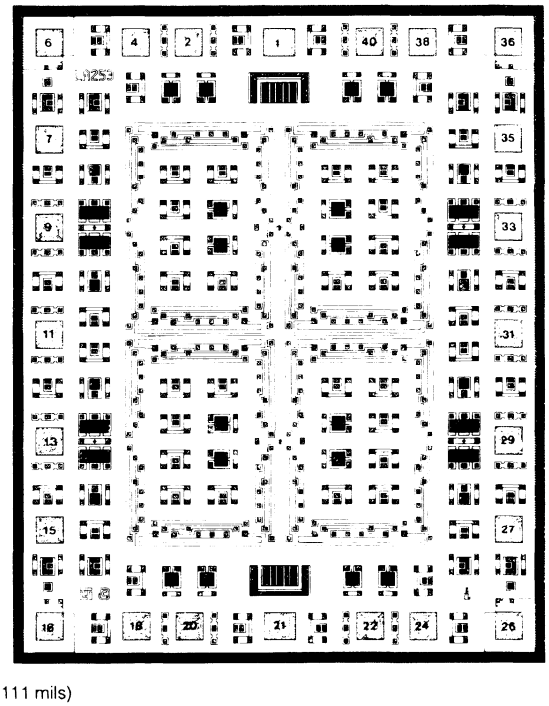
LA251 (SIZE 150 x 144 mils)
Maximum number of bonding pads available - 40

MODULA LA250 SERIES ARRAY LAYOUT



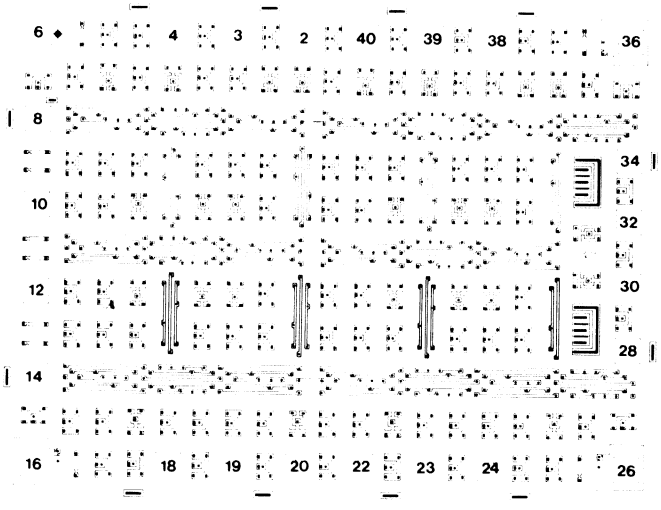
LA252 (SIZE 151 x 111 mils)
Maximum number of bonding pads available - 32

MODULA LA250 SERIES ARRAY LAYOUT



LA253 (SIZE 92 x 111 mils)
Maximum number of bonding pads available - 24

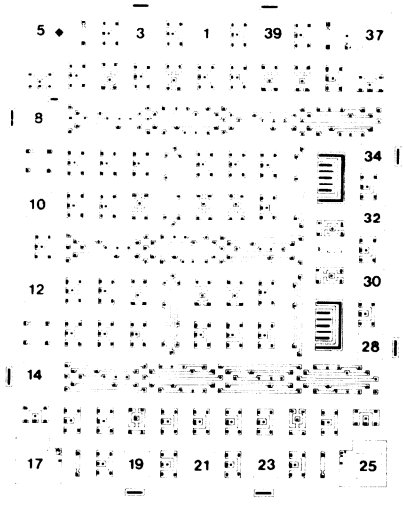
MODULA LA250 SERIES ARRAY LAYOUT



LA201 (SIZE 127 x 94 mils)

Maximum number of bonding pads available - 24

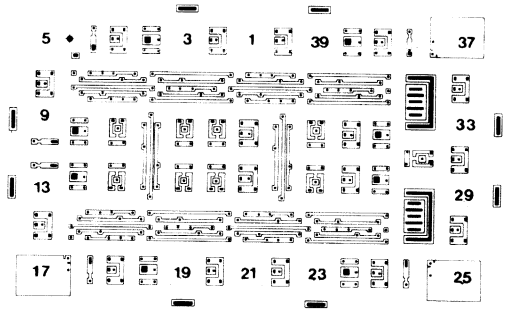
LA200 SERIES ARRAY LAYOUT



LA202 (SIZE 78 x 94 mils)

Maximum number of bonding pads available - 18

LA200 SERIES ARRAY LAYOUT



LA204 (SIZE 56 x 91 mils)

Maximum number of bonding pads available - 18

LA200 SERIES ARRAY LAYOUT

SCD 1

BiFET PRODUCTS

BD data sheets

BA application notes

GENNUM CORPORATION

LC508 Class A Amplifier with 3 Independent Gain Blocks

DATA SHEET

FEATURES

- 1 μV input referred noise
- 1.0 to 5 VDC operating range
- 73 dB typical gain (adjustable)
- 0.28 to 2.0 mA range of transducer current
- 1% electrical distortion
- the first and second blocks, or second and third blocks can be DC coupled
- 100 Hz to 50 kHz frequency response
- suitable for active filtering

ABSOLUTE MAXIMUM RATINGS

Parameter	Value / Units
Supply Voltage	5 VDC
Power Dissipation	25 mW
Operating Temperature	-10 to +40°C
Storage Temperature	-20 to +75°C

TYPICAL ELECTRICAL CHARACTERISTICS

(refer to test circuit and conditions))

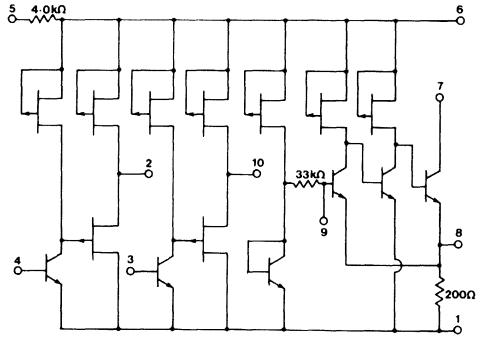
PARAMETER	MIN	TYP	MAX	UNITS
Gain (Closed Loop)				
S1,S2 Closed	69	73	77	dB
Distortion	-	1	4	%
Amplifier Current				
(I_A+I_{MIC})	160	245	340	μA
Transducer Current (I_L)				
S3 Closed	1.1	1.3	1.7	mA
S3 Opened	200	275	350	μA
Input Referred Noise	-	1	2	μV
Stable with Battery				
Resistance (R_B) to:	-	-	22	Ω
Input Bias (I_B)				
Note 2,3,& 4	-50	0	50	nA

DESCRIPTION

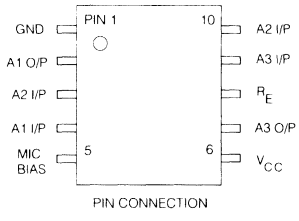
The LC508 is a 10 pin Class A amplifier utilizing Gennum's proprietary low voltage bipolar JFET technology. It consists of 3 single ended, low noise inverting gain blocks. The first blocks have a minimum open loop gain of 40 dB, typically 50 dB. The closed loop gain is set by the ratio of the feedback resistor to the impedance of the source resistance. When the microphone is used as the source, the gain is set by the ratio of the gain trim resistor R_{FA} to the microphone impedance (see application circuit). If a telecoil is switched in, which typically has half the impedance of the microphone, the gain is increased by approximately 6 dB. This results in a higher sensitivity for the telecoil. The third block is an open collector output transistor with the bias being set by R_E.

Typically, the gain of the first 2 blocks is set to 25 dB each, with the third block at 23 dB, giving a total gain of 73 dB.

Gain trim can be accomplished with the use of a feedback resistor on the first block, while the volume control is used as the feedback control on the second block. This gives a volume control range greater than 40 dB.



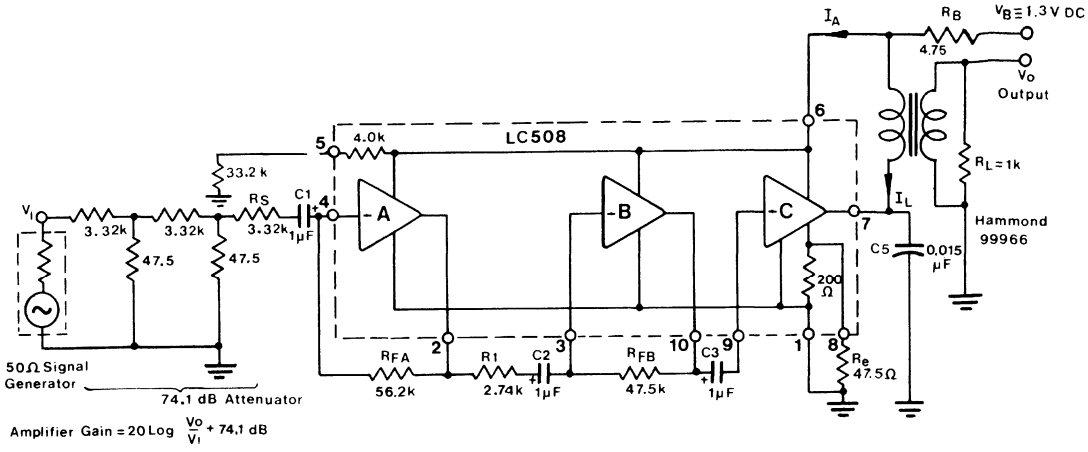
FUNCTIONAL SCHEMATIC



PIN CONNECTION

BD 1

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991



All external resistors in ohms & ±1% tol., all capacitors in µF & ±10% tol. unless otherwise stated

NOTES:

1. Amplifier gain = 20 Log $\frac{Vo}{V1}$ + 74.1dB
2. To calculate I_B for stage A, measure $V1$ with $S1$ open $I_B = \frac{V1}{1.056\ M\Omega}$
3. To calculate I_B for stage B, measure $V2$ with $S2$ open $I_B = \frac{V2}{1.047\ M\Omega}$
4. For $V1$ and $V2$ measurements a high impedance DCVM must be used (>1 GΩ).

Fig. 1 Test Circuit

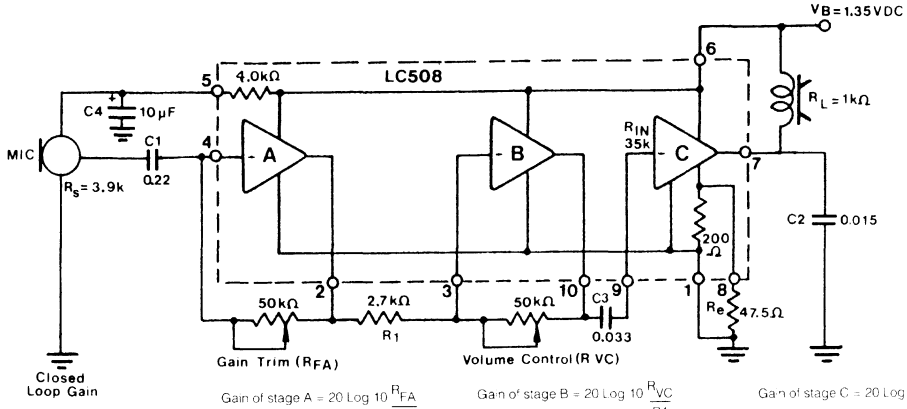
The tone control for the LC508 is calculated by using the input capacitor($C1$) and the source impedance (R_S) as the RC network, except for the third block, where it can be calculated by the input impedance (R_{IN}) and the input capacitor ($C3$).

The open loop output impedance for blocks A and B are approximately 7 Ω.

AVAILABLE PACKAGING
10 pin PLID®, MINIpac,
MICROpac & SLT

TEST CONDITIONS

PARAMETER	VALUE / UNITS
V_B	1.3 V DC
Source Impedance	3.36 kΩ
Frequency	1 kHz
Output Level	0.5 V RMS
Load Impedance	1 kΩ
Noise Filter Bandwith at 12dB/oct	0.2 - 10 kHz
Ambient Temperature	25 °C



All resistors in ohms, all capacitors in µF unless otherwise stated

Fig. 2 Typical Hearing Aid Circuit

GENNUM CORPORATION

Class A Compression Amplifier

LD511 DATA SHEET

FEATURES

- 64 dB typical electrical gain
- 0.94 VDC voltage regulator
- 7 ms attack time, 40 ms release time
- 15 dB threshold adjustment
- low noise and distortion
- compression ratio ∞ : 1
- 0.3 kHz - 6 kHz frequency response

ABSOLUTE MAXIMUM RATINGS

Parameter	Value / Units
Supply Voltage	2.4 V
Power Dissipation	25 mW
Operating Temperature	-10 to +40°C
Storage Temperature	-40 to +75°C

TYPICAL ELECTRICAL CHARACTERISTICS

(refer to test circuit)

PARAMETER	VALUE			
COMPRESSION INACTIVE (S1 OPEN)	MIN	TYP	MAX	UNITS
Gain	60	64	68	dB
Input Referred Noise	-	2.0	4.0	mV
Total Harmonic Distortion +Noise	-	1	3	%
Amplifier Current (I_A)	-	0.4	0.6	mA
Transducer Current (I_L)	1.35	1.6	2.0	mA
Input Impedance	-	15	-	kΩ
Regulated Voltage Output	0.90	0.96	1.0	VDC
COMPRESSION ACTIVE (S1 CLOSED)				
Compression Range	-	∞	-	dB
Total Harmonic Distortion + Noise ($V2$ = 1 mV)	-	4.0	7.0	%
Attack Time ($V2$ switched from 112 µV to 2 mV)	-	7	-	ms
Release Time	-	40	-	ms
Compression Output ($V2$ = 1 mV)	-	0.10	0.18	VRMS

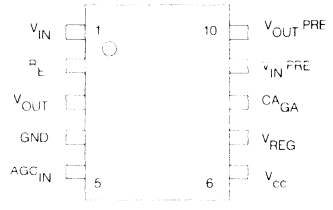
DESCRIPTION

The LD511 is a Class A compression amplifier which can operate over a range of DC battery voltages from 1.1 V to 2.4 V. A voltage regulator, which is independent of supply voltage variations, is on-chip to supply a stable 0.94 VDC bias to the amplifier circuitry and to the microphone.

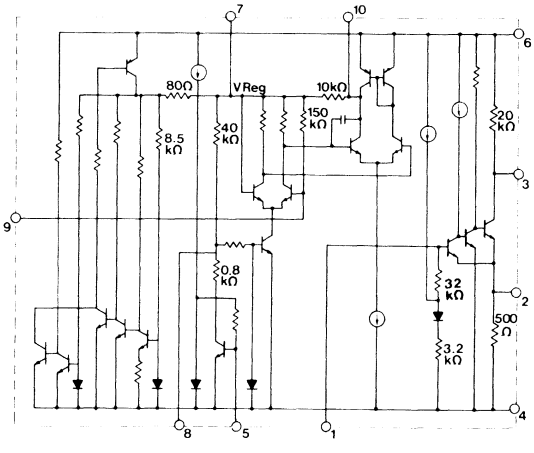
The LD511, in compression, has approximately 15 dB of threshold adjustment by varying R_f (see application circuit) and a compression function ratio of ∞ : 1.

Attack and release times are fixed at a ratio of 7 ms and 40 ms respectively and they can be adjusted simultaneously by changing the filter capacitor on pin 8.

The output stage bias can be set to accomodate different receiver impedances by changing the value of R_E. The voltage across R_E (pin 2 to ground) is a constant 27 mV so the bias current is 27 mV divided by the total value of R_E in parallel with 500 Ω.



PIN CONNECTION



FUNCTIONAL SCHEMATIC

BD 2

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

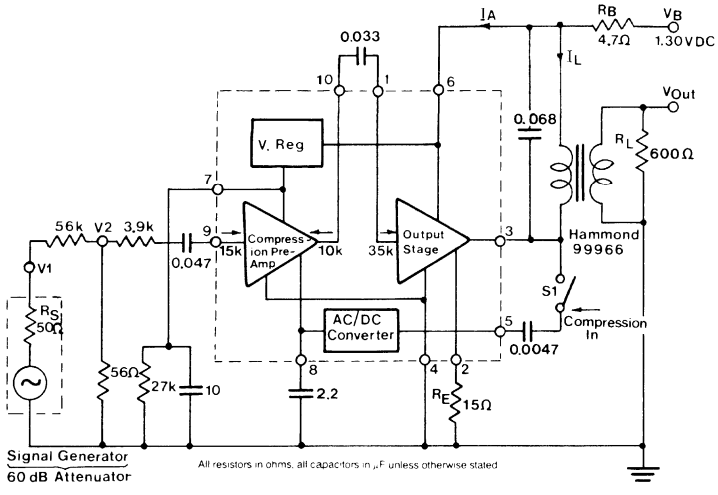


Fig.1 Test Circuit

TEST CONDITIONS

PARAMETER	VALUE / UNITS
SupplyVoltage	1.30 VDC
Test Frequency	1.0 kHz
Signal Source Impedance	3.9 kΩ
Output Testing Level	0.50 VRMS
Noise Filter Bandwidth at -12 dB/oct.	0.2 - 10 kHz
Ambient Temperature	25 °C
Battery Resistance	4.7 Ω

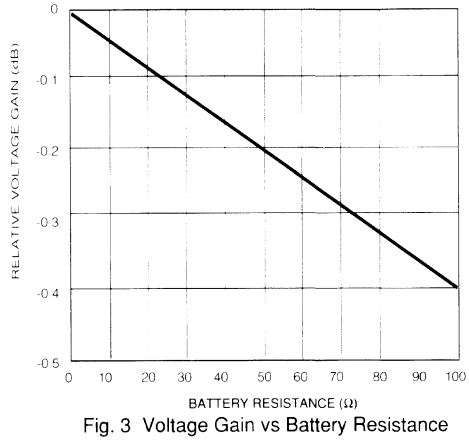


Fig. 3 Voltage Gain vs Battery Resistance

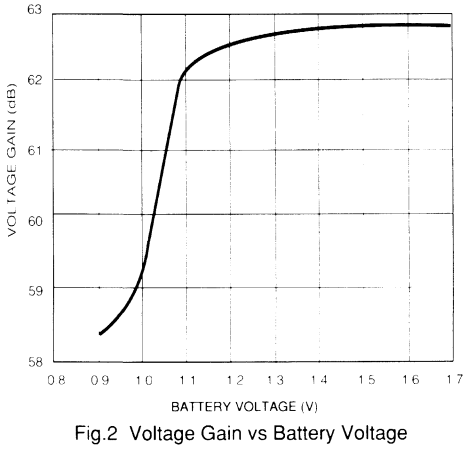


Fig.2 Voltage Gain vs Battery Voltage

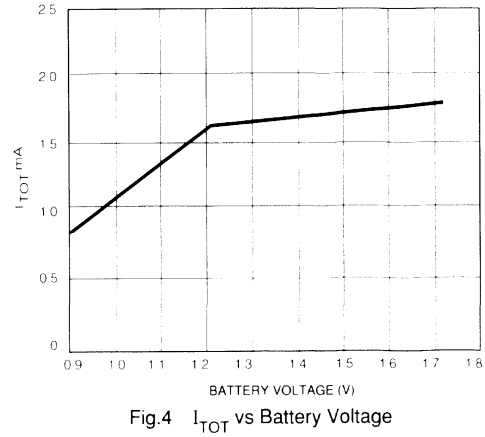


Fig.4 I_{TOT} vs Battery Voltage

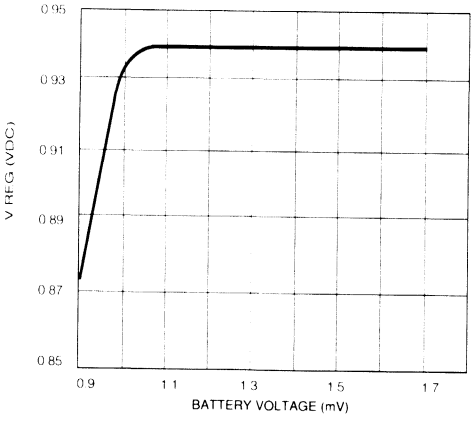


Fig.5 Voltage Regulator vs Battery Voltage

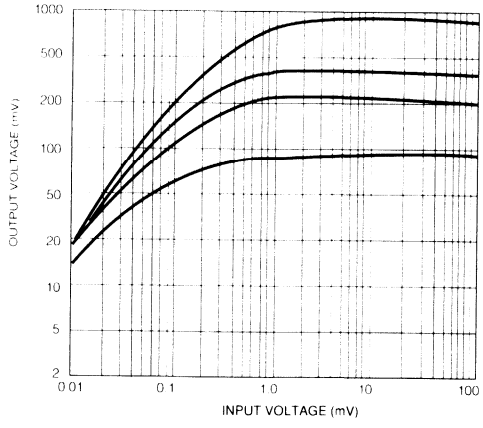


Fig.7 Threshold Adjustment

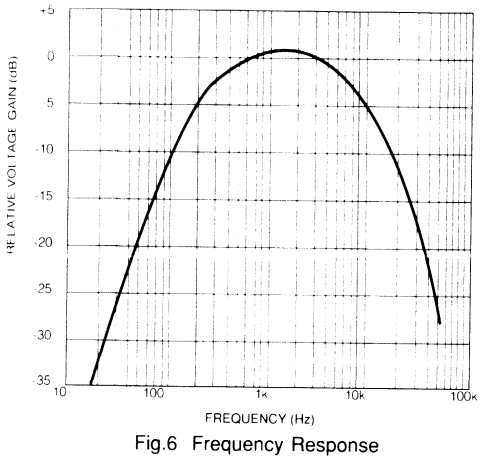


Fig.6 Frequency Response

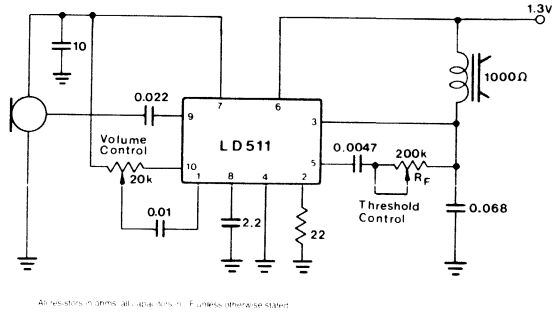
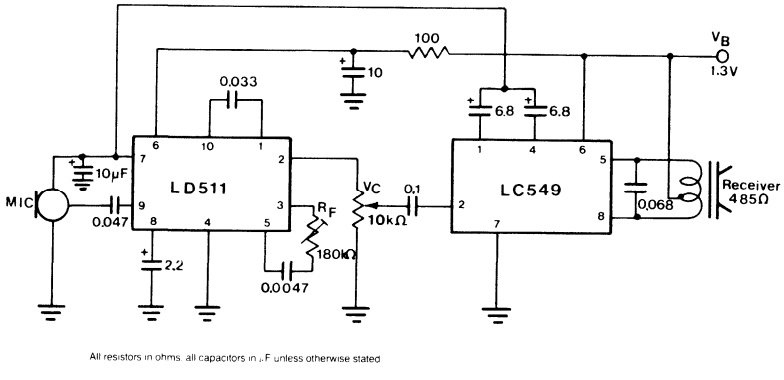


Fig.8 LD511 Stand Alone

BD 2



AVAILABLE PACKAGING
10 pin MICROpac,
PLID*, MINIpac and SLT

Fig.9 LD511 / LC549 Configured for Reduced Start Up Transients on the LC549

GENNUM CORPORATION

High Power, Class B Output Stage - LC551

DATA SHEET

FEATURES

- adjustable gain to 48 dB
- capable of driving low impedance receiver (110 Ω)
- low component count, 3 small capacitors and 1 resistor
- gain trim can be used as volume control for reduced noise
- minimal start - up transient
- frequency bandwidth of 18 kHz

TYPICAL ELECTRICAL CHARACTERISTICS

(refer to test circuit and conditions)

PARAMETER	MIN	TYP	MAX	UNITS
Gain	46	48	50	dB
Gain Expansion	-	-	3	dB
Quiescent Current:				
Amplifier	120	210	335	µA
Transducer	120	220	405	µA
Total	240	430	740	
Input Referred Noise	-	1.3	2.5	µV
Total Harmonic Distortion				
at V_O = 0.707 V RMS	-	1.2	2.5	%
at V_O = 1.3 V RMS	-	3	5.2	%
Stable with battery resistance to	-	22	-	Ω

DESCRIPTION

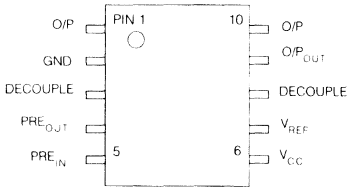
The LC551 is a 10 pin low voltage, class B amplifier which operates over a battery voltage range of 1.1 V DC to 3 V DC.

The LC551 consists of three gain blocks. The first block is an inverting amplifier with the gain set by two external resistors. This gain trim feature can be used as a volume control in hearing aid applications. The second block is an inverting unity gain amplifier which serves as a phase splitter. The outputs from the first and second blocks drive the differential inputs of the third block. The third block has a fixed AC gain of 28 dB when driving a receiver.

This amplifier has internal compensation eliminating the need for a capacitor across the receiver. Two ground pins are available for "*star*" grounding to reduce any second harmonic distortion produced by ground line resistance.

ABSOLUTE MAXIMUM RATINGS

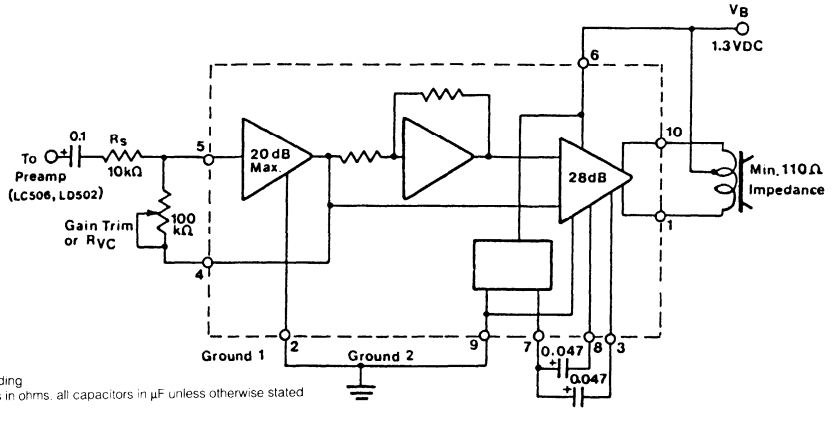
Parameter	Value / Units
Supply Voltage	5 V DC
Operating Temperature	-10 to + 40 °C
Storage Temperature	-40 to + 75 °C



PIN CONNECTION

BD 3

FUNCTIONAL BLOCK DIAGRAM



Patent Pending
All resistors in ohms, all capacitors in µF unless otherwise stated

Document No. 500 - 77 - 4

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

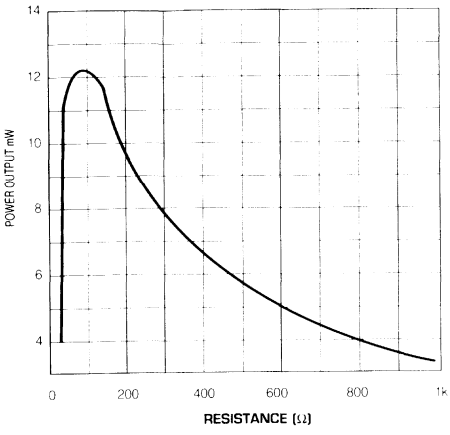


Fig. 1 Power Output vs Load Resistance at 7% Distortion $R_B = 0$ $V_B = 1.35$ V

TEST CONDITIONS

PARAMETER	VALUE / UNITS
V_B	1.3 V DC
R_S	10 kΩ
Frequency	1 kHz
Output Level for Gain	0.707 VRMS
Gain Expansion	1.3 VRMS
Load Impedance	400 Ω
Noise Filter Bandwith at 12 dB/oct	0.2-10 kHz
Ambient Temperature	25 °C
R_B	4.7 Ω
R_{VC}	100 kΩ

NOTES: 1. To measure noise, point A is grounded.

2. Output impedance is typically 8 Ω with V_{OUT} = 0.5 VRMS

3. Gain expansion =Gain (at 1.3 VRMS output) - Gain (at 0.707 VRMS output)

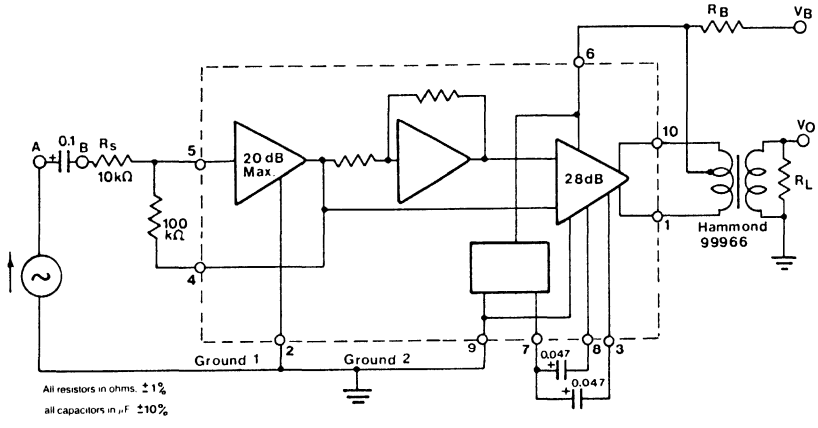


Fig. 2 Test Circuit

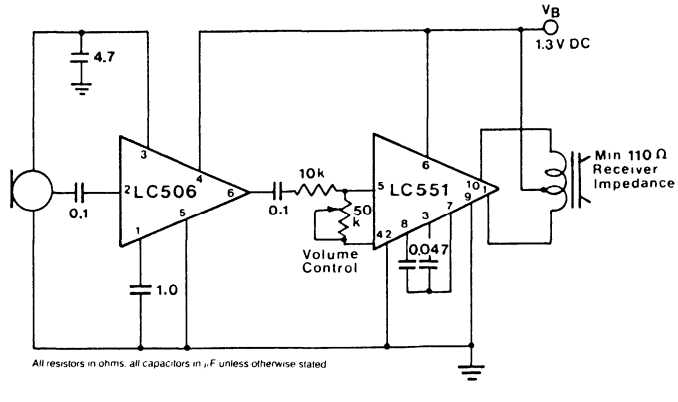


Fig. 3 Typical Hearing Aid Circuit

AVAILABLE PACKAGING

10 pin PLID*, MICROpac, & SLT

GENNUM CORPORATION

Dual, Continuous, Analog Highpass Filter - LF580

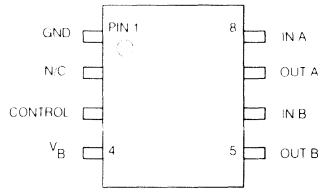
DATA SHEET

FEATURES

- only 2 small capacitors required
- 200 to 10 kHz adjustable corner frequency
- dual 12 dB/oct Butterworth filter (24 dB/oct cascaded)
- 1.1 to 3.0 VDC operating range
- adjustable by a single potentiometer

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value / Units
Power Supply	V_B	5V DC
Storage Temperature	T_{STG}	-40 °C to 100 °C



PIN CONNECTION

DESCRIPTION

The LF580 continuous analog filter consists of two second order (12 dB/oct), tunable (0.2 to 10 kHz) highpass Butterworth filter blocks.

Tracking and corner frequency of each block are controlled by a single potentiometer. Cascading the two blocks together results in a single 24 dB/oct. high pass filter requiring only two external 0.001 µF capacitors for the filter response, and one external 0.1 µF output capacitor.

An automatic high pass filter can be developed with the LF580. Controlling the current from pin 3 to ground either by a variable resistor, or a transistor current sink will allow electronic control of the filter corner frequency. The voltage at pin 3 is typically fixed at 18 mV.

The output noise of each filter stage is typically 5.6 µV. Cascading the two filter blocks together will produce a noise level which is

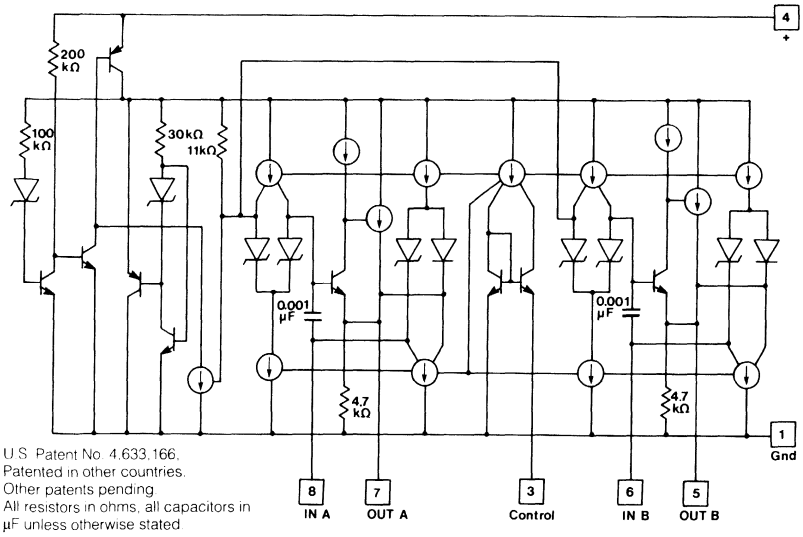
$$V_N = \sqrt{(V_{N1})^2 + (V_{N2})^2} \text{ or } 8\ \mu V$$

Where V_N is the total output noise of both filters, V_{N1} and V_{N2} is the noise of each filter.

To improve the signal-to-noise ratio of the filter the LF580 should be placed after a preamplifier, provided that the signal level does not exceed the maximum signal handling capability of 50 mVRMS.

BD 4

FUNCTIONAL SCHEMATIC



U.S. Patent No. 4,633,166.
Patented in other countries.
Other patents pending.
All resistors in ohms, all capacitors in µF unless otherwise stated.

AVAILABLE PACKAGING
8 pin PLID*, MINIpac, MICROpac & SLT

Document No. 500 - 73 - 5

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

TEST CONDITIONS

(measured at 25 C). Refer to Test Circuit

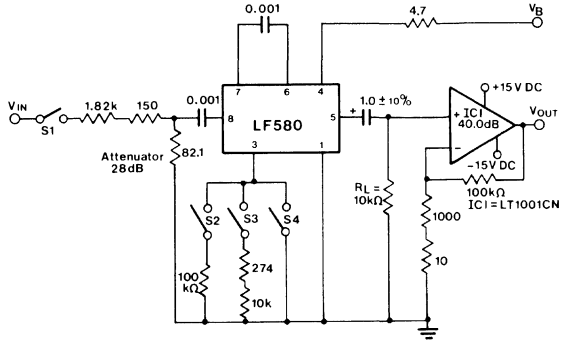
Parameter	VB (V DC)	Frequency	V_{IN}	Close Switch	Procedure and Formula to Determine Parameter
Insertion Loss (dB)	1.30	1 kHz	1 VRMS	S1, S2	I Loss = 20 Log (V_{OUT} / V_{IN}) -12
Current/Drain	1.30	N/A	N/A	S4	N/A
CornerFrequency	1.30	1 kHz	1 VRMS	A) S1, S2 B) S1, S3	A -Measure output voltage $V_{OUT\ 1}$. B -Measure output voltage $V_{OUT\ 2}$ f_c = 1000 ($V_{OUT\ 1}$ / $V_{OUT\ 2}$)
Distortion	1.30	1 kHz	1.250 VRMS	S1, S2	Measure Distortion
Output Noise	1.30	N/A	N/A	S2	OutputNoise = V_{OUT} / 1000 (Filter Bandwidth 200 Hz- 10 kHz @ -12 dB / Oct.)
Supply Rejection	3.0*	N/A	N/A	S2	S.R. = 20 Log(V_{OUT}) - 40

*NOTE: with 1 VRMS Modulation @ 1kHz.

ELECTRICAL CHARACTERISTICS

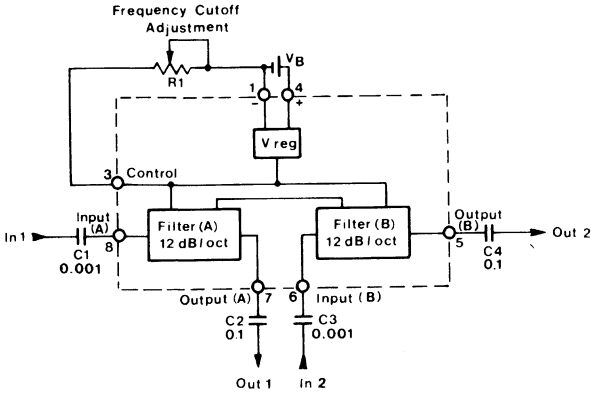
(Refer to Test Circuit and Conditions)

Parameter	Min.	Typ	Max.	Units
Insertion Loss		2	3	dB
Current Drain (I_T)	200	280	370	µA
Output Noise (filters combined)		8	10	µV
Total Harmonic Distortion		2	5	%
Supply Rejection		45	56	dB
Corner Frequency	1300	1650	1900	Hz



NOTES: 1) Tolerances of all resistors and capacitors are ±1%.
2) All switches are normally open unless otherwise stated.
3) ICI = LT1001CN low noise operational amplifier.
4) All resistors in ohms, all capacitors in µF unless otherwise stated.

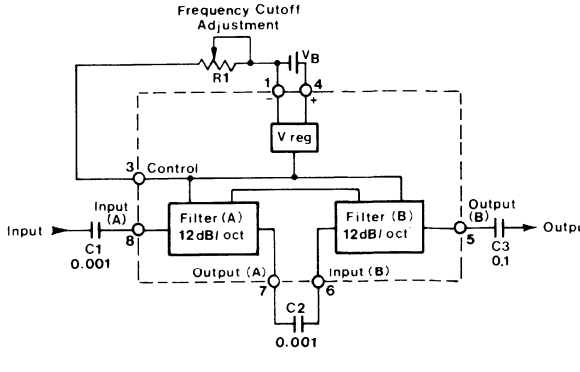
Fig. 1 Test Circuit



Applications: 1. 24 dB per Octave Filter variable high pass (manual)
2. Automatic High Pass Filter
3. Dual 12 dB per Octave Filter variable high pass

NOTES: Corner Frequency (fc) adjusted by R1 at -24 dB / oct from 200 Hz to 10 kHz
C1 = C2 = 0.001 for Filter Response
All resistors in ohms, all capacitors in µF unless otherwise stated

Fig. 2 Dual High Pass Filter



NOTES: Corner Frequency (fc) adjusted by R1 at -24 dB / oct from 200 Hz to 10 kHz
C1 = C2 = 0.001 for Filter Response
All resistors in ohms, all capacitors in µF unless otherwise stated

Fig.3 High Pass Filter

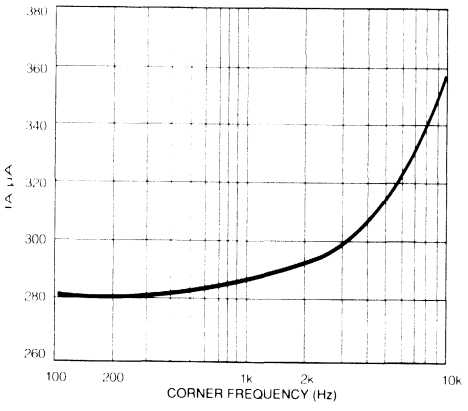


Fig. 4 LF580 Current Drain

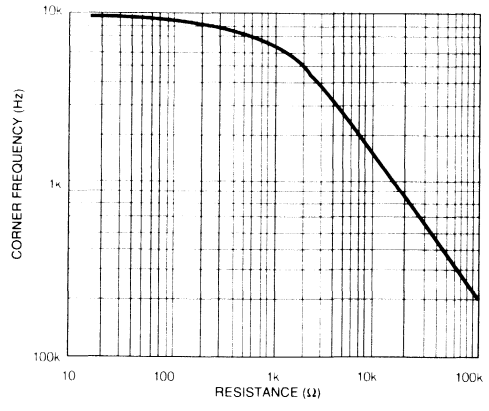
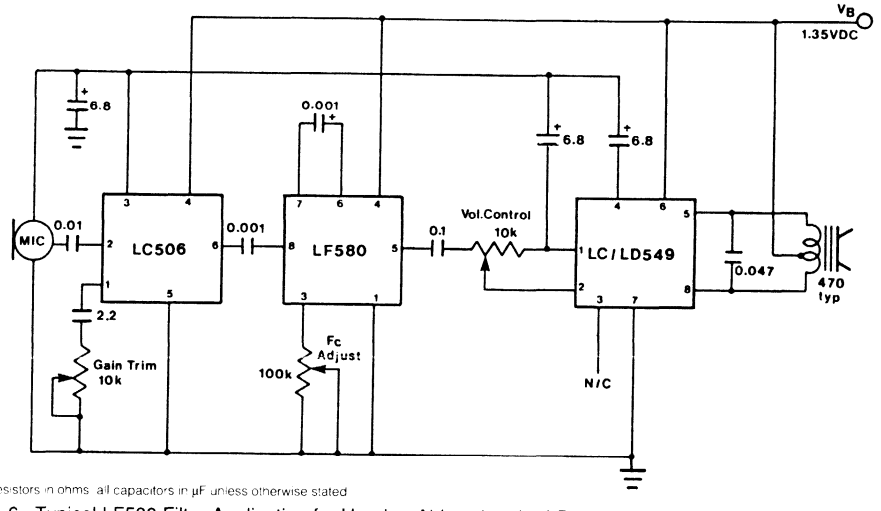
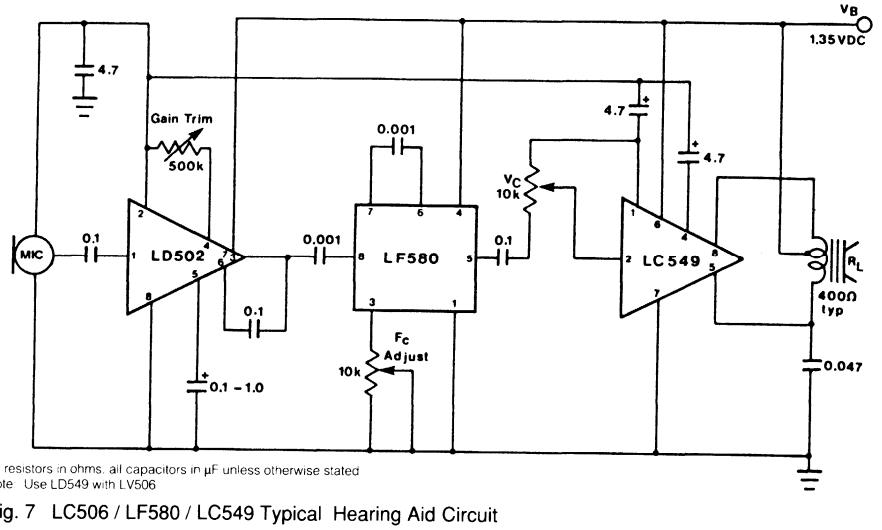


Fig. 5 LF580 Corner Frequency Adjustment



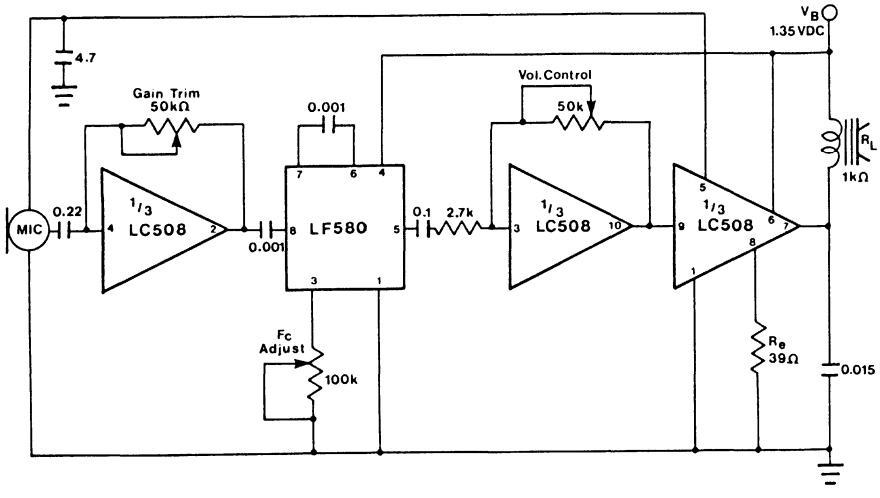
All resistors in ohms, all capacitors in µF unless otherwise stated

Fig. 6 Typical LF580 Filter Application for Hearing Aids using the LD502 & LC549



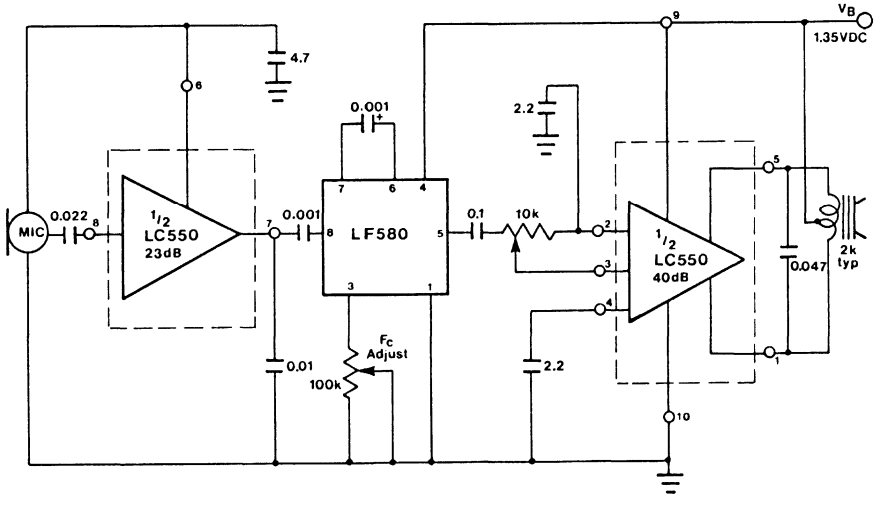
All resistors in ohms, all capacitors in µF unless otherwise stated
Note: Use LD549 with LV506

Fig. 7 LC506 / LF580 / LC549 Typical Hearing Aid Circuit



All resistors in ohms, all capacitors in μF unless otherwise stated

Fig. 8 LF580 / LC508 Typical Hearing Aid Circuit



All resistors in ohms, all capacitors in μF unless otherwise stated
Note: 2.2 μF when receiver's ≥ 3kΩ

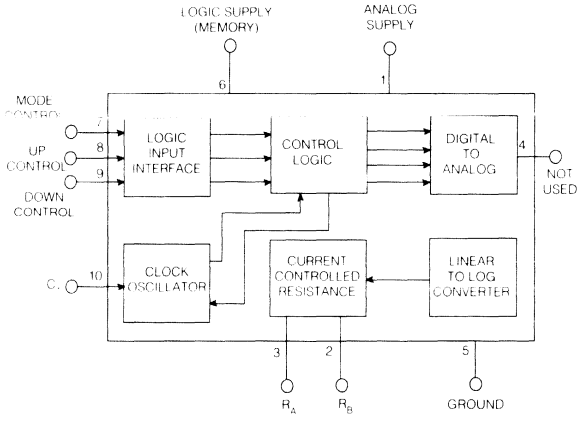
Fig. 9 LF580 / LC550 Typical Hearing Aid Application

Digitally Controlled Transconductance Block

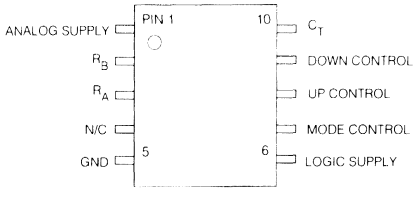
GT560/LV560 DATA SHEET

FEATURES

- 1.0 to 5V DC supply voltage
- 70μA of analog current drain (typical)
- 6μA of memory current drain (typical)
- single or dual switch control
- touch plate compatible (for GT560 on 30MΩ typ impedance)
- typical 42dB range
- adjustable clock frequency increases or decreases time required to change diode impedance



FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTION

CIRCUIT DESCRIPTION

The GT/LV560 is a low voltage transconductance block which can be used as an electronic volume control. The transconductance element consists of two diodes back-to-back, whose impedance is varied by changing the amount of current through the diodes.

The impedance of the diodes is controlled by digital circuitry which consists of:

- an oscillator with an external capacitor, C_T, to set the ramp frequency f_c.

$$f_c = \frac{5 \times 10^{-7}}{C_T}$$

- logic interface, which senses the volume up-down controls
- a digital / analog converter
- the control logic/debounce logic
- synchronous up-down counter

To increase or decrease the LV560 impedance, the switching mechanism can be touch sensitive contacts or a mechanical switch. In either configuration, the switches are connected from pin 8 to ground and pin 9 to ground. Any resistance, up to 6 MΩ from pin 8 or 9 to ground will activate the GT/LV560 control circuitry and the device will change impedance levels.

OPERATION

The impedance can be controlled using one of two methods. The first method utilizes a Single Pole Single Throw (SPST), momentary contact switch which combines the up/down function in one action (see Fig. 2). The second method (see Fig. 3) uses one Single Pole Double Throw (SPDT), or two SPST switches which provide a separate action for the up-down function. These switches can be mechanical or touch sensitive.

To operate the GT/LV560 using a single switch, the Mode Control (MC) is connected to the positive supply, the switch will then act in an alternating manner first increasing impedance when activated, then decreasing impedance when activated a second time, both at a rate determined by the external timing capacitor.

If separate UP or DOWN switches are used, the Mode Control pin connects to ground. Making contact to the DOWN switch, the diode impedance will decrease until the switch is released or the diodes reach minimum impedance (4kΩ). Similarly, contact to the UP switch will increase the diodes impedance until the switch is released or the maximum value of diode impedance has been reached (500kΩ).

BD 5

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Once the minimum (4 kΩ) or maximum (500 kΩ) impedance is reached and the switch is still closed, the impedance will stop changing until the switch is released and the direction is reversed. Should both switches be closed simultaneously, the output impedance will remain unchanged.

In order for the LV560 to be activated and change impedance the switch must be pressed for at least one time constant, t_c.

where $t_c = \frac{1}{f_c}$

Normally the timing capacitor C_T, is connected to ground, as shown in Figure 1. When the circuit is turned on, C_T is required to charge from 0 VDC to approximately 0.56 VDC. During this charge up condition, the clock is disabled and ramping of the impedance by the touch contacts or switches will be inactive until C_T is charged.

Small values of C_T eg. 0.1 µF, will cause a time delay of less than 2 seconds, however as the value of C_T is increased, eg. 1.0 µF the charge time can be as high as 20 seconds.

If the length of the charge time is undesirable, the capacitor can be referenced to a microphone decoupling point as shown in Figure 13. In this configuration the capacitor charge time will be less than 2 seconds with a 1.0 µF capacitor.

It is required that C_T be connected to a positive reference voltage which has a high supply line rejection ratio, such as a voltage regulator, or a microphone decoupling point. If C_T was referenced directly to the supply, any battery line signals greater than 10 mVRMS will affect the clock rate on the GT/LV560. This would cause the ramp speed to become erratic as the impedance is being changed.

When the hearing aid is initially turned on, e.g. insertion of the battery , the diode impedance will be at a random setting for the LV560 and a mid gain setting (which is typically 7 steps from the minimum impedance setting) for the GT560. Once the desired impedance is determined this value will be held constant by the memory circuitry on the LV560. Connecting the memory supply (VM), to the battery positive bypassing the on-off switch, will allow the volume control to retain the selected impedance even with the hearing aid switched off. The memory current drain is extremely low at 6 µA. If however the battery is removed, memory will be lost.

The 560 may be used as the feedback impedance across an inverting gain block, such as a LC508 preamplifier. The gain of the amplifier would then be determined by the ratio of the diode impedance to the source impedance of the LC508 preamplifier. For example, if a microphone with a typical impedance of 4 kΩ were to be used as the source to the LC508 preamplifier, and the GT/LV560 connected across the input and output pins with a minimum impedance of 4 kΩ, the minimum gain would be a ratio of 4:4 (or 0 dB).

With the maximum impedance at 500 kΩ, the maximum gain would be a ratio of 500:4 approximately (or 42 dB). The volume control range is 42 dB.

It is important that either R_A or R_B on the LV560 be DC coupled to the LC/LP508 preamplifier stage to set up a reference voltage on the diodes, otherwise the volume control will not be biased properly. The LV560 pins R_A and R_B, will operate from 200 mV below supply to 500 mV above ground.

Note: A resistor of 1.2 MΩ is required between Pin 2 and Pin 3 to limit the step size to 3.0 dB. If this resistor is not used at high gain settings the steps will be greater than 3.0 dB, resulting in high distortion on the LC/LP508.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	5 VDC
Power dissipation at $T_A \leq 70°C$	25 mW
Operating Temperature	-10°C to +40°C
Storage Temperature	-20°C to +70°C

ELECTRICAL CHARACTERISTICS

(refer to test circuit and test conditions)

Parameter	Min	Typ	Max	Units
I_{Analog}	40	70	130	µA
I_{Logic}	-	6	10	µA
Distortion	-	1	2.9	%
Step Size	1.0	2.5	4.0	dB
Impedance :				
Low	2.5	4	6	kΩ
High	250	500	700	kΩ
VCO	36	42	48	dB

TEST CONDITIONS (refer to test circuit)

Parameter	Value	Units
Supply Voltage	1.3	VDC
Source Impendance	3.94	kΩ
Frequency	1.0	kHz
Output Level for		
Impedance Test	15	mVRMS
Distortion	10	mVRMS
Temperature	25	°C

TEST PROCEDURES

1) I_{Analog} measured with the 560 impedance set to minimum.

2) To calculate the minimum impedance, set the LV560 to lowest impedance setting.

$$V_{OUT} = 15 \text{ mV and measure } V_{IN}$$

$$Z_{MIN} = \frac{V_{OUT}\,(3.94k)}{V_{IN}}$$

3) To calculate Z_{MAX} set the impedance of the 560 to maximum.

Set the output (V_{OUT}) to 15 mV and measure V_{IIN}

$$Z_{MAX} = \frac{V_{OUT}\,(3.94k)}{V_{IN}}$$

NOTE:
S1 and *S2*
- for GT560, is referenced to the power supply
- for the LV560, is referenced to ground

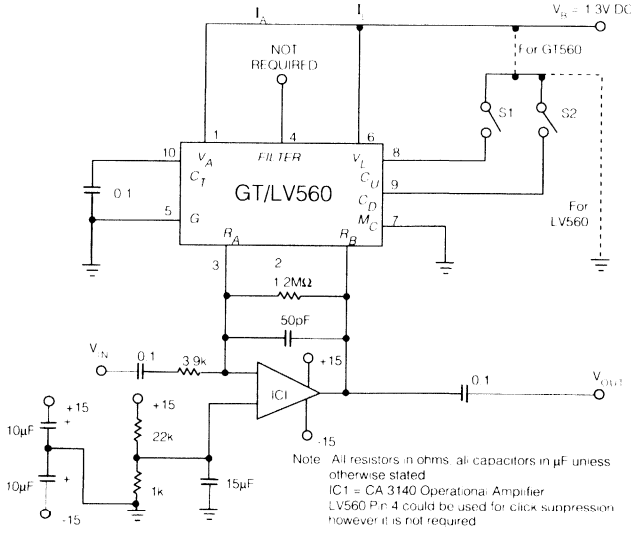


Fig.1 LV560 Test Circuit

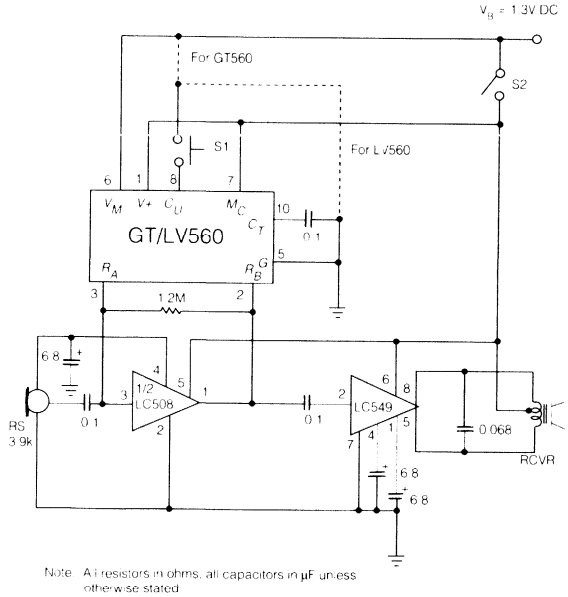


Fig.2 Typical Hearing Aid Circuit

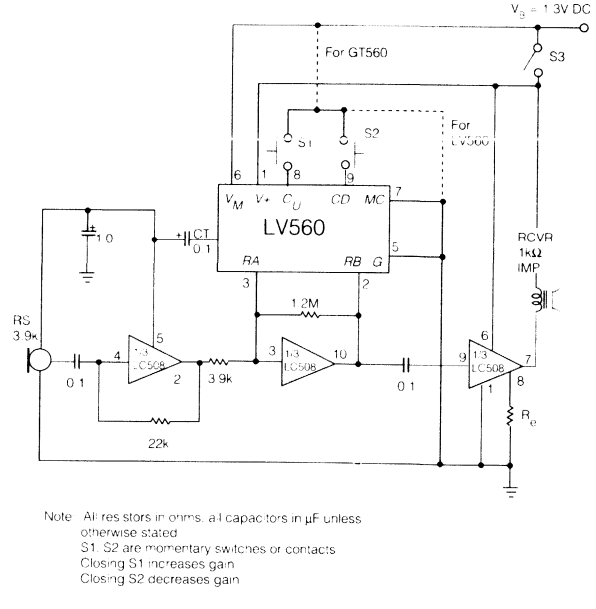


Fig.3 Typical Hearing Aid Application

BD 5

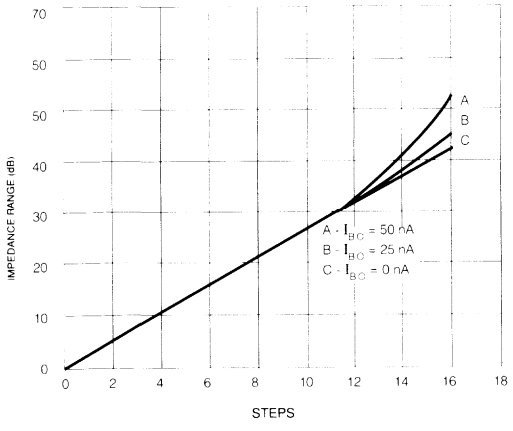
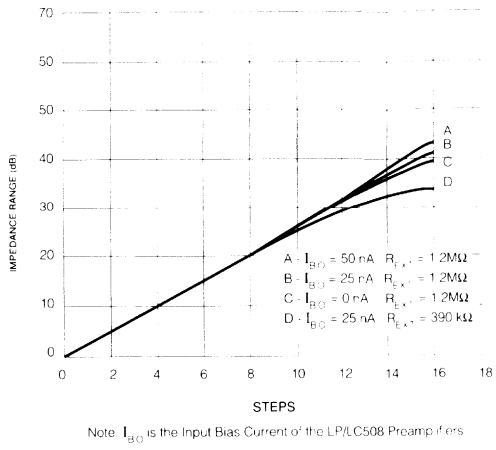


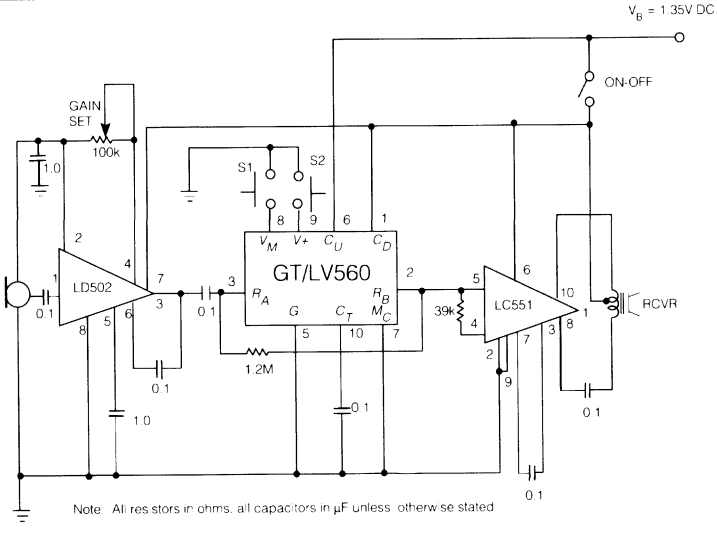
Fig.4 Output Impedance Characteristics without External Shunt Resistor



Note: I_{BIC} is the Input Bias Current of the LP/LC508 Preamplifiers

Fig.5 Output Impedance Characteristics with R_{EXT} = 1.2 MΩ

AVAILABLE PACKAGING
10 pin MICROpac,
PLID*, and SLT



Note: All resistors in ohms, all capacitors in µF unless otherwise stated

Fig.6 LD502/LV560/LC551 Typical Application

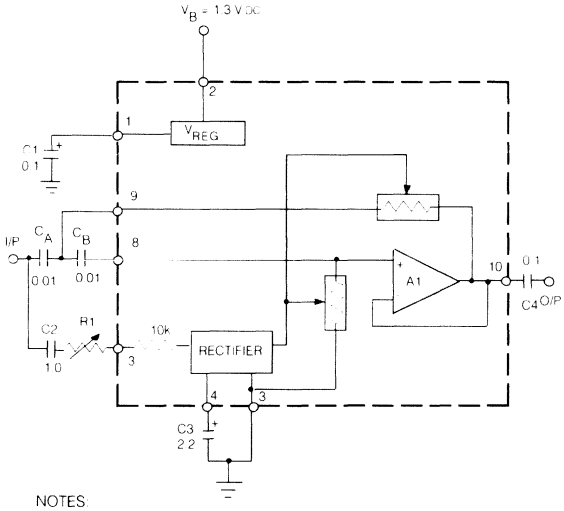
GENNUM CORPORATION

Adaptive Highpass Filter
LF581

DATA SHEET

FEATURES

- unity gain 12 dB/oct. highpass Butterworth filter
- adaptive frequency range from 200 Hz to 2 kHz
  (limits are adjustable, but remain one decade apart)
- rectifier threshold set to 82 dBSPL* (adjustable)
- low noise, typically 3 μV
- typically 260 μA current drain
- operates from 1.1 to 3VDC



NOTES:

1. To change corner frequency limits, the values of C_A and C_B are increased or decreased.
   R1 sets the threshold.
   Pins 5 and 6 are not connected.

* 2. Using a microphone with a sensitivity of -60 dBV / μB at 1kHz

3. All resistors in ohms, all capacitors in μF unless otherwise stated.

FUNCTIONAL BLOCK DIAGRAM

AVAILABLE PACKAGING
10 pin PLID* & MICROpac
8 pin DIP

DESCRIPTION

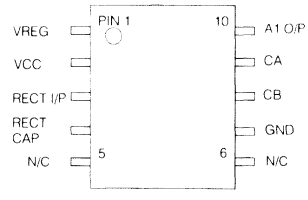
The LF581 level-sensitive, adaptive highpass filter reduces low frequency noise with respect to increasing input levels. On-chip, the LF581 is comprised of a current controlled highpass filter, a half-wave rectifier, and a voltage regulator for microphone bias.

The internal rectifier senses the long term average signal level and controls the filter response by setting the control current to the filter. The rectifier input threshold has been set to 82 dBSPL (2.5 mVRMS) and the sensitivity, with respect to the input signal, can be increased by placing a preamplifier gain, such as the LC/LP508 preamplifier, before the rectifier.

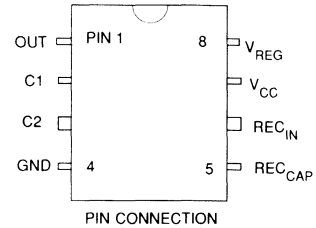
Important features of the LF581 are attack and release times, set to 30 ms and 90 ms respectively or higher, providing a time frame by which to discriminate between short term average speech levels and long term average noise levels. The average time period of a speech frame is about 15 ms which is not long enough to activate the filter, however long term average noise, which can have time periods greater than 30 ms, will activate the filter provided that the amplitude is above the rectifier threshold.

An increase of 20 dB above this threshold will automatically increase the corner frequency one decade above the initial corner frequency. The filter will only allow an increase in corner frequency of one decade, regardless of further increases in the input signal level.

BD
6



PIN CONNECTION
10 pin PLID* & MICROpac



PIN CONNECTION
8 PIN DIP

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LF581 ELECTRICAL CHARACTERISTICS

(Refer to test conditions and test circuit)

PARAMETER	MIN.	TYP.	MAX.	UNITS
I_{TOT}	145	280	395	µA
V_{REG} (Pin 1)	0.870	0.925	0.990	Vdc
Rect Input (Pin 3)	0.490	0.580	0.670	Vdc
Rect Filter (Pin 4)	0.490	0.580	0.670	Vdc
Pin 8 Voltage (Vp8)	0.550		0.780	Vdc
Pin 9 Voltage (Vp9)	0.550		0.780	Vdc
Filter Insertion Loss	0	1	1.3	dB
Distortion		2	3	%
Rectifier Gain	4	6	8	
I_{D0}	0.700	1.0	1.3	µA
I_{RANGE}	8	10	12	
Slope	0.75	1.0	1.25	
V_{THL} (Rect. threshold)	1.96	2.5	3.2	mVdc
f_C	140	200	260	Hz
Max. I/P Signal (5%THD)		65		mVRMS
Output noise		3		µV
Attack Time		15		ms
Release Time		45		ms

ELECTRICAL TEST CONDITIONS

PARAMETER	VALUE	UNITS
Frequency (VAC1, VAC2)	1.0	kHz
Temperature	25	°C
Output Level for:		
Insertion Loss (S1 closed)	85	mVRMS
Distortion (S1 closed)	85	mVRMS
Input Level for:		
Rectifier Gain (S2 closed)		
AC2	10	mVRMS
AC2	18	mVRMS

DC MEASUREMENTS:

For I_{D0} -Close S3 and Measure I_{A1} as I_{D0}
(VDC2 = 0 Vdc)

I_{D3} -measure Pin 4 DC Voltage ($V_{PIN\,4}$)
-set VDC1 to = 180 mVdc + $V_{PIN\,4}$
-close S4
-close S3 and measure I_{A1} as I_{D3}

I_{D1} measure $V_{PIN\,4}$ dc
-set VDC1 = 35 mVdc + $V_{PIN\,4}$
-close S4
-close S3 and measure I_{A1} as I_{D1}

I_{D2} -measure $V_{PIN\,4}$ DC
-set VDC1 = 85mVdc + VP4
-close S4
-close S3 and measure I_{A1} as I_{D2}

Slope of Filter = $\frac{I_{D2} - I_{D1}}{0.05}$ x 14K

RECTIFIER GAIN:

-Close S2
-set VAC2 = 10 mVRMS
-measure $V_{PIN\,4}$ as Vm1
-set VAC2 = 18 mVRMS
-measure $V_{PIN\,4}$ as Vm2

Rectifier Gain = 2 x (Vm1 - Vm2)

RECTIFIER THRESHOLD:

V_{THL} = VAL/RECTIFIER GAIN x SLOPE

$V_{AL} = (V_{PIN\,4} + 85mV) - ((I_{D2}-I_{D0})/SLOPE) \times 14K$

CORNER FREQUENCY (f_C):

-set VDC2 = 18mV + $V_{PIN\,9}$
-measure I_{a1} as I_a
-set VDC2 = $V_{PIN\,9}$ - 18mV
-measure I_{a1} as I_b

$$I2 = \frac{3 \times (I_{DO} + I_a)}{4 - (I_{D0} + I_b)}$$

$$f_C = \frac{432844000}{(1/I_{D0}) + 1/(I2 - I_{D0})}$$

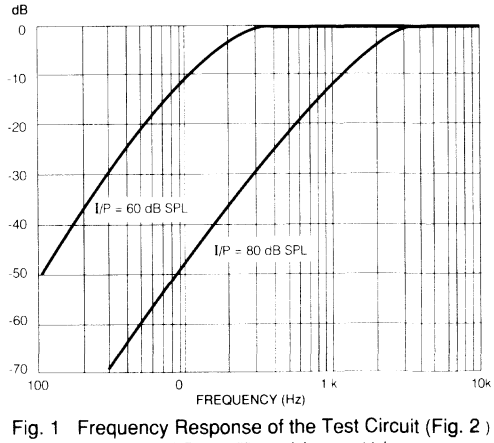


Fig. 1 Frequency Response of the Test Circuit (Fig. 2)
(with a 20 dB Preamplifier and the output taken from Pin 10 of the LF581)

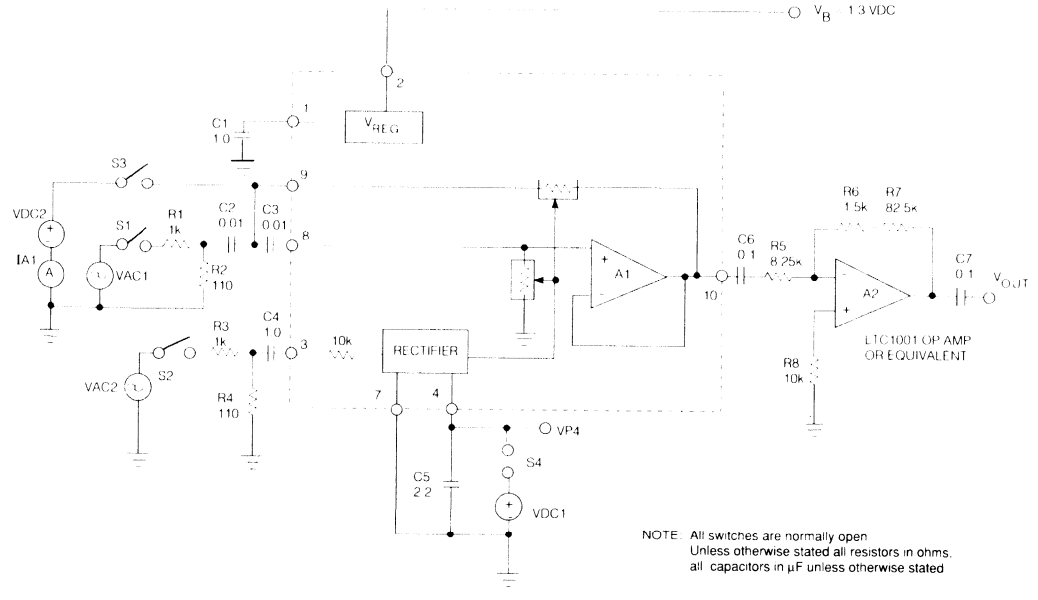


Fig.2 LF581 Test Circuit

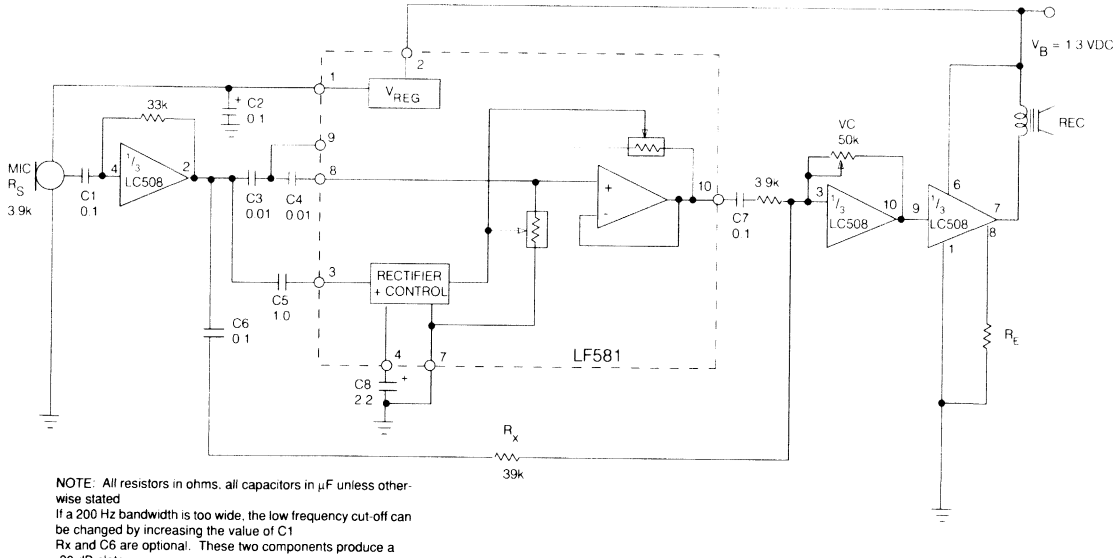


Fig. 3 LP508/LF581 Typical Application Circuit

GENNUM CORPORATION

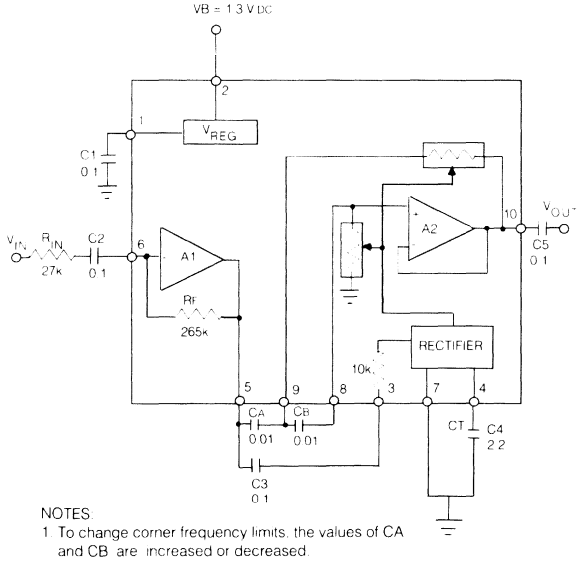
Adaptive Highpass Filter with Independent Gain Block

LS581 TENTATIVE DATA SHEET

FEATURES

- unity gain 12 dB/oct. highpass Butterworth filter
- adaptive frequency range from 200 Hz to 2 kHz
  (limits are adjustable, but remain one decade apart)
- rectifier threshold set to 82 dBSPL (adjustable) see note 2
- low noise, typically 3 µV
- I_T typically 300 µA
- operates from 1.1 to 2 VDC
- preamplifier with 45 dB open loop gain

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. To change corner frequency limits, the values of CA and CB are increased or decreased.
2. Using a microphone with a sensitivity of -60dB / µB @ 1kHz
3. All resistors in ohms, all capacitors in µF unless otherwise stated

DESCRIPTION

The LS581 level-sensitive, adaptive highpass filter reduces low frequency noise with respect to increasing input levels. The LS581 is comprised of a current controlled highpass filter, a half-wave rectifier, a voltage regulator for microphone bias and a separate preamplifier.

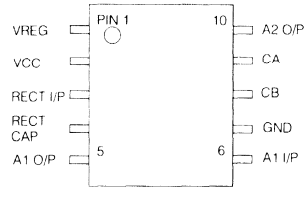
The internal rectifier senses the long term average signal level and controls the filter response by setting the control current to the filter.

The rectifier input threshold has been set to 82 dBSPL (2.5mVRMS) and the sensitivity, with respect to the input signal, can be increased by placing the internal preamplifier (A1) before the LS581. The preamplifier has a minimum open-loop gain of 45 dB and includes an internal 265 kΩ feedback resistor from its input to its output, to facilitate in setting the gain.

An important characteristic of the LS581 is the proper setting of the attack and release times. It is recommended that the attack and release times are set to 30 ms and 90 ms respectively. This provides a time frame by which to discriminate between short term average speech levels and long term average noise levels. The average time period of a speech frame is about 15 ms which is not long enough to activate the filter, however long term average noise, which can have time periods greater than 30 ms, will activate the filter providing that the amplitude is above the rectifier threshold.

BD 7

An increase of 20 dB above this threshold will automatically increase the corner frequency one decade above the initial corner frequency. The filter will only allow an increase in corner frequency of one decade, regardless of further increases in the input signal level.



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LS581 ELECTRICAL CHARACTERISTICS

(Refer to test conditions and test circuit)

PARAMETER	MIN.	TYP.	MAX.	UNITS
I_{TOT}	165	300	450	µA
V_{REG} (Pin 1)	0.870	0.925	0.990	VDC
Rect Input (Pin 3)	0.490	0.580	0.670	VDC
Rect Filter (Pin 4)	0.490	0.580	0.670	VDC
Pin 8 Voltage ($V_{PIN\ 8}$)	0.550		0.780	VDC
Pin 9 Voltage ($V_{PIN\ 9}$)	0.550		0.780	VDC
Pin 5 Voltage ($V_{PIN\ 5}$)	0.490		0.670	VDC
Filter Insertion Loss	0	1	1.3	dB
Distortion		2	3	%
Rectifier Gain	4	6	8	
I_{D0}	0.700	1.0	1.3	µA
I_{RANGE}	8	10	12	
Slope	0.75	1.0	1.25	
V_{THL} (Rect. threshold)	1.96	2.5	3.2	mVdc
f_C	140	200	260	Hz
A1 Open Loop Gain	45			dB
R_F	175	265	355	kΩ
A1 I_{SOURCE}	-55		-15	µA
A1 I_{SINK}	15		100	µA
Max. I/P Signal(5% THD)	65			mV_{RMS}
Output noise		3		µV
Attack Time		15		ms
Release Time		45		ms

ELECTRICAL TEST CONDITIONS

PARAMETER	VALUE	UNITS
Frequency (VAC1, VAC2)	1.0	kHz
Temperature	25	°C
Output Level for:		
Insertion Loss (S2 closed)	85	mV_{RMS}
Distortion (S2 closed)	85	mV_{RMS}
Input Level for:		
Rectifier Gain (S2 closed)		
AC2	10	mV_{RMS}
AC2	18	mV_{RMS}
AC Open Loop Gain (S5 closed)		
AC1	75	mV_{RMS}

DC MEASUREMENTS:

For I_{D0} -Close S3 and Measure I_{A1} as I_{D0}
(VDC2 = 0 Vdc)

I_{D3} -measure Pin 4 DC Voltage ($V_{PIN\ 4}$)
-set VDC1 to = 180 mVdc + $V_{PIN\ 4}$
-close S4
-close S3 and measure I_{A1} as I_{D3}

I_{D1} -measure $V_{PIN\ 4}$DC
-set VDC1 = 35 mVdc + $V_{PIN\ 4}$
-close S4
-close S3 and measure I_{A1} as I_{D1}

I_{D2} -measure $V_{PIN\ 4}$DC
-set VDC1 = 85mVdc + VP4
-close S4
-close S3 and measure I_{A1} as I_{D2}

Slope of Filter = $(I_{D2}-I_{D1}) / 0.05 \times 14K$

RECTIFIER GAIN:

-Close S2
-set VAC2 = 10 mV_{RMS}
-measure $V_{PIN\ 4}$ as Vm1
-set VAC2 = 18 mV_{RMS}
-measure $V_{PIN\ 4}$ as Vm2

Rectifier Gain = 2 x (Vm1 - Vm2)

RECTIFIER THRESHOLD:

V_{TH} = VAL/RECTIFIER GAIN x SLOPE
$V_{AL} = (V_{PIN\ 4} + 85mV) - ((I_{D2}-I_{D0})SLOPE \times 14K$

CORNER FREQUENCY (f_C):

-set VDC2 = 18mV + $V_{PIN\ 9}$
-measure I_{A1} as I_a
-set VDC2 = $V_{PIN\ 9}$ - 18mV
-measure I_{A1} as I_b

$$I2 = \frac{3 \times (I_{DO} + I_a)}{4 - (I_{D0} + I_b)}$$

$$f_C = \frac{432844000}{\frac{1}{I_{D0}} + \frac{1}{I2 - I_{D0}}}$$

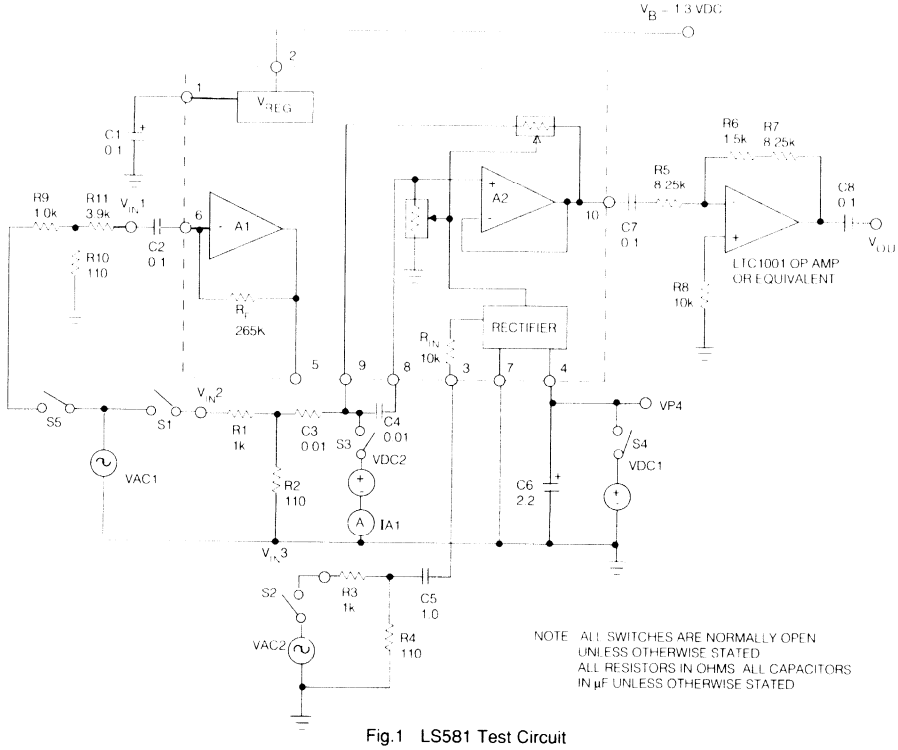


Fig.1 LS581 Test Circuit

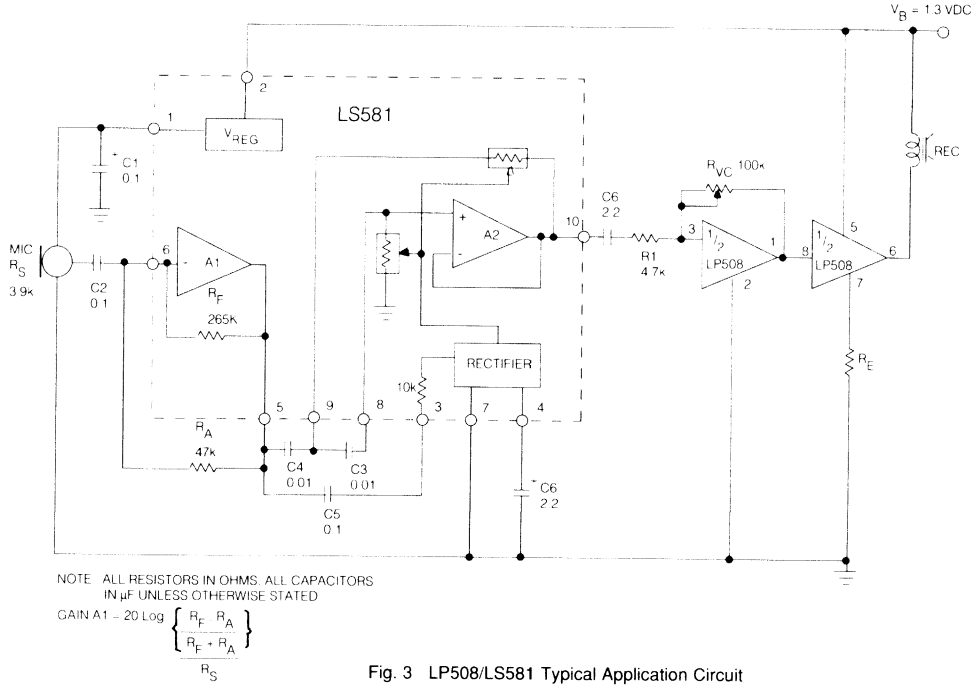


Fig. 3 LP508/LS581 Typical Application Circuit

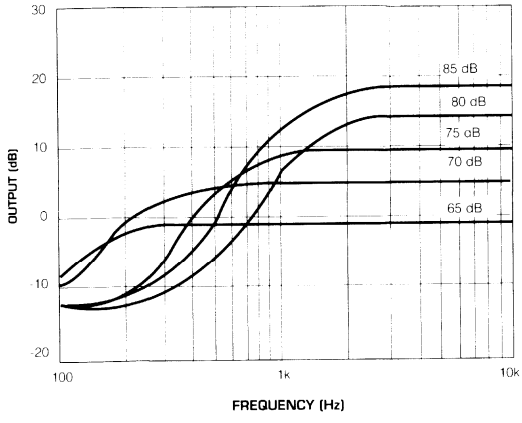


Fig. 3 LS581 Frequency Response (with 20 dB Preamplifier)

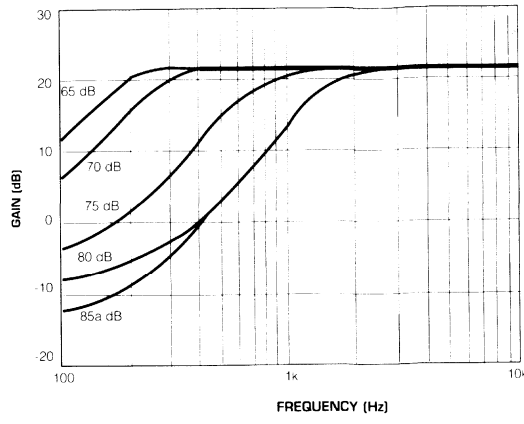


Fig. 4 LS581 Gain Curve (with 20 dB Preamplifier)

AVAILABLE PACKAGING

10 pin PLID*, MICROpac
& MINIPAC

INTRODUCTION

The 508 family of Class A amplifiers are presently offered in either an 8 pin or 10 pin version, which utilize Gennum's proprietary low voltage BiFET technology. This relatively new technology allows these amplifiers to operate with lower currents and increased supply rejection.

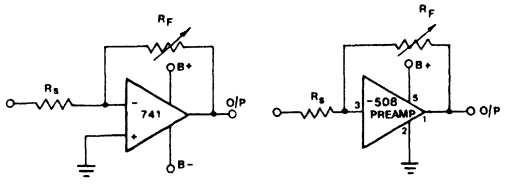
CIRCUIT DESCRIPTION

The LP508 is the 8 pin version consisting of a preamplifier, a 4 kΩ microphone decoupling resistor, and an output stage with a 27 mV reference voltage at the emitter of the output stage (R_e pin).

The LC508 is a 10 pin device which contains 2 preamps, a 4 kΩ microphone decoupling resistor and an output stage with a 54 mV reference voltage at the emitter of the output stage (R_e pin). Access to pin R_e allows the manufacturer to set the amount of bias current flowing through the receiver for maximum efficiency.

The preamps found on both the LP508 and the LC508 can be compared to an operational amplifier. Most rules that apply to op-amps also apply to the preamp of a 508.

The negative input of an ideal op-amp would appear as a virtual ground when used as an inverting amplifier. This is also the case with the input of a 508 preamp. Any impedance or resistance connected to the input pin becomes the equivalent input impedance of the preamplifier, as with the industry standard op-amp of Fig.1a. Fig.1b shows how a 508 preamp performs the same function, while only requiring a single polarity power supply.



a. General Purpose Op - Amp b LP508 Preamp

Fig.1 Op-Amp Equivalent Circuit vs 508 Preamp Equivalent Circuit

The gain of an inverting amplifier can be determined by the ratio of the feedback resistor (R_F) to the source impedance (R_s). The gain (A_v) in dB can be calculated by the following formula :

$A_V = 20 \log R_F / R_S$ for $A_V << A_{vol}$ where A_{vol} = open loop gain

Typically the open loop gain (A_{vol}) of a 508 preamp is 45 dB. Knowing this value is important when calculating the gain of an amplifier, because closed loop gain must always be lower than open loop-gain. It is recommended that the maximum closed loop gain be 20 dB lower than the open loop gain. If the closed loop gain is less than 20dB from the open loop gain, the gain should be calculated by:

$$A_{vcl} = \frac{A_{vol}}{1 + A_{vol} \times \frac{R_s}{R_F}}$$

A_{vcl} = Closed Loop Gain

The preamplifier has an open loop output impedance of typically 7 kΩ. When the preamplifier feedback loop is closed, the output impedance will be reduced by the difference between open loop gain and closed loop gain ($A_{vol} - A_{vcl}$). eg., if ($A_{vol} - A_{vcl}$) = 20 dB, or 10 times lower, the closed loop output impedance would be 700 Ω.

The 508 preamp and output stages are internally bias compensated preventing any DC current flow, via the volume control (feedback resistor), into or out of the input terminals of the device. No internal biasing would result in an audible scratchiness during changes in volume control settings. This also allows DC coupling between stages because the inputs and outputs of all stages have identical DC voltage levels.

Since no op-amp is ideal, a residual amount (± 50nA maximum) of bias current could flow. Coupling between any two stages is possible without any appreciable DC voltage or current offset being created at the output.

BA 1

OUTPUT STAGE

The current drive output stage of the 508 family is also an inverting amplifier. It is a unity gain voltage follower from the input to the R_e pin. The DC voltage at pin R_e is determined by an internally fixed reference voltage. This reference voltage, in conjunction with R_e, sets the bias current flowing through the receiver.

For the LP508, $I_{BIAS} = 27 \text{ mV}/R_t$

LC508, $I_{BIAS} = 54 \text{ mV}/R_t$ Where $R_t = R_e // R_{ext}$

The maximum input level that the output stage of the LP508 can handle is 27 mV peak. Since the LC508 output stage emitter (R_e pin) is referenced at 54 mV, it can handle input levels as large as 54 mV peak before limiting occurs.

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Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

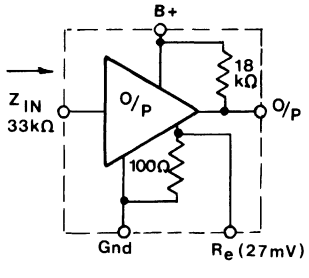
It is also important to know the maximum output drive capabilites of the 508 preamps. The maximum source current on the output of the preamps is typically 30μA ± 45%. This means that once R_F is reduced to 1k Ω, the maximum peak voltage that the preamp can swing , at its output before limiting, is:

$$V = I \times R$$
$$= 30\mu A \times 1k\Omega$$
$$= 30mV\ peak$$

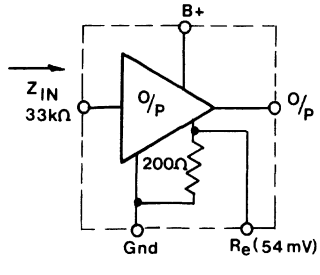
Once R_F goes below 1kΩ, the preamp will become the limiting factor and not the output stage. On the LP508 the output limiting voltage of the output stage is 27mV peak and a 1kΩ feedback resistor would be the limit before the preamp saturates prior to the output stage. As for the LC508, the limit resistor would be 2kΩ because the peak output limiting voltage of the output stage is higher, at 54mV.

It was necessary on the LP508, that an internal 18kΩ resistor be placed on the collector of the output stage because of instability resulting from positive feedback (from output to input) and receiver impedance characteristics. This resistor limits the maximum gain of the amplifier.

The LC508 is an inverting amplifier, using negative feedback from input to output, therefore no output stage collector resistor is necessary. Input impedance of the output stage on both LC and LP508 is typically 33kΩ . Knowing this impedance value makes calculating the output stage low-end frequency response straightforward.



LP508 Output Stage.



LC508 Output Stage

Fig.2

EFFECTS OF VARYING MICROPHONE IMPEDANCE

Since the tolerance of the output impedance of a Knowles microphone could vary by up to $\approx \pm$ 4.7dB, and the closed loop gain of the preamp is dependant upon microphone output impedance, gain can also vary.

One way to reduce the effect of gain variance, (due to microphone impedance tolerances) is to use a resistor in series with the microphone.

e.g. If an 18kΩ series resistor is used, the gain variation range will change from ±4.7dB down to ±1dB. The only disadvantage to this method is that at room temperature the 18kΩ resistor has about 2.44μV of noise associated with it.

To calculate total noise use :

$$N = \sqrt{n1 + n2}$$

where n1 is 2.44μV for an 18kΩ resistor and n2 is 4μV of microphone noise (26dB).

Therefore, overall system noise can increase from 4μV to 4.68μV with the addition of an 18kΩ series resistor.

FREQUENCY SHAPING

Because all input and output pins are accessible to the designer, frequency shaping can be easily achieved in many different areas of the amplifier.

Starting at the input of the preamp, a tone control can be achieved by using a capacitor value, selected for the desired corner frequency.

For low - end frequency filtering, (high pass filter), the -3dB break point is calculated by:

$$f_C(-3dB) = \frac{1}{2 \times \pi \times R_S \times C_{IN}}$$

Where R_S is the source impedance, (usually the output impedance of a microphone), and C_{IN} is the input coupling capacitor.

e.g. if $R_S = 3.5k\Omega$ and $C_{IN} = 0.1\mu F$

$$\text{the } f_C(-3dB) = \frac{1}{2 \times \pi \times R_S \times C_{IN}}$$

$$= \frac{1}{2 \times \pi \times (3.5k\Omega) \times (0.1\mu F)}$$

$$= 455Hz$$

Another accessible point for filtering is between the preamp and output stage. The input impedance (Z_{IN}) of the output stage is known to be 33k Ω therefore

$$f_c = \frac{1}{2 \times \pi \times (Z_{IN}) \times (C2)}$$

where Z_{IN} is the input impedance of the output stage and C2 is the coupling capacitor to that stage. Because of the nature of the current drive output stage, low pass filtering can be achieved at the output stage collector by placing a capacitor in parallel with the reciever. This is sometimes called peak shifting and is shown in Fig. 3.

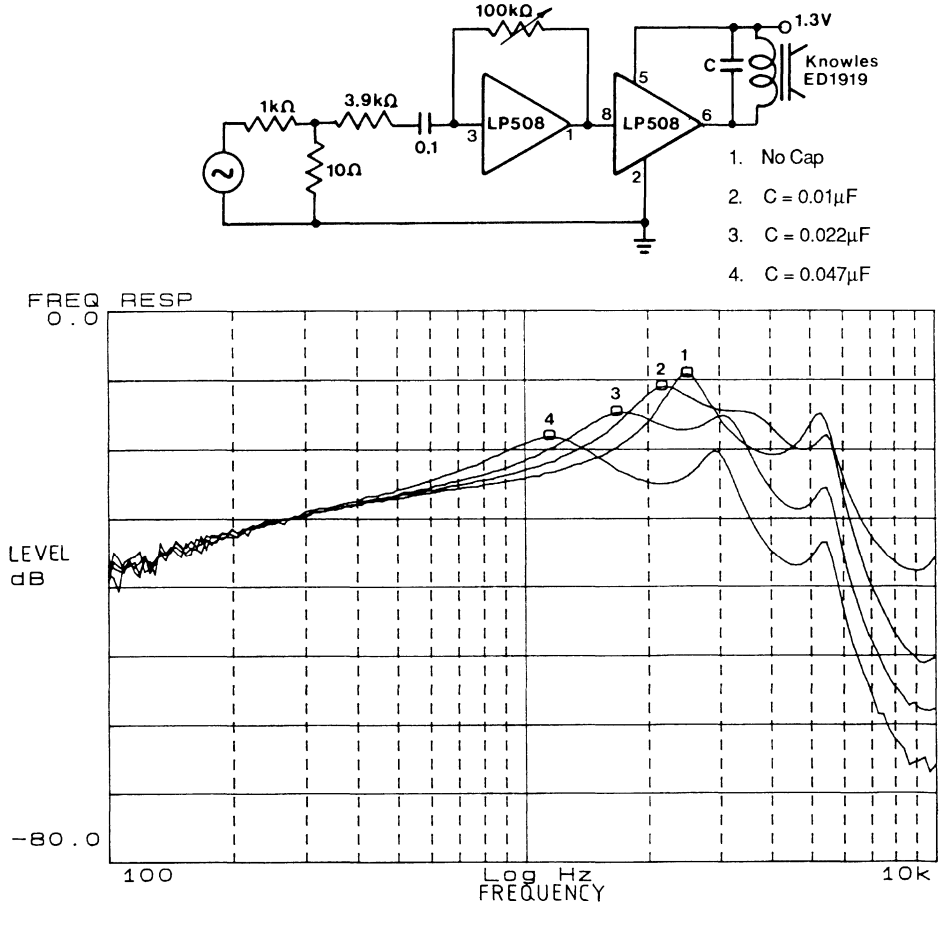


Fig. 3. Peak Shifting using a Parallel Capacitor.

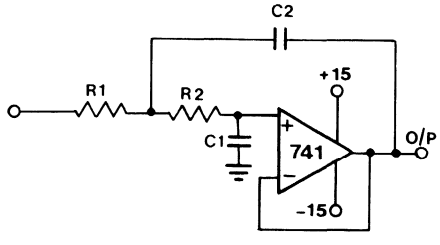
ACTIVE FILTERING TECHNIQUES

MULTIPLE FEEDBACK FILTERS

The most common type of higher - order active filter designs involves the use of operational amplifiers. The 508 family of ICs can be used to design multiple feedback active filters. Detailed calculations and a more in depth understanding of active filterings available in Gennum 600-9 article on Active Filtering for Hearing Aids.

ACTIVE BUFFER FILTERS

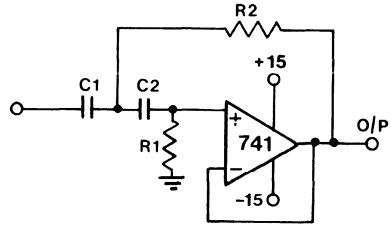
The output stage of a 508 may also be used as an active buffer filter, similar to an op-amp non-inverting buffer circuit. The following buffer circuits are designs using general purpose operational amplifiers (741). The same filters can be designed using the 508 output stage.



$R1 = R2$
$C2 = 2C1$

$$f_c = \frac{1}{2 \times \pi \times R1 \times C1 \times \sqrt{2}}$$

Fig. 4 Low Pass Filter using a General Purpose Op-Amp.

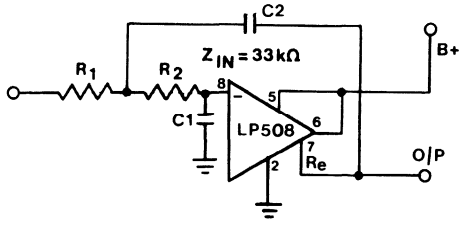


$C1 = C2$
$R1 = 2R2$

$$f_c = \frac{1}{2 \times \pi \times R1 \times C1 \times \sqrt{2}}$$

Fig. 5 High Pass Filter using a General Purpose Op-Amp

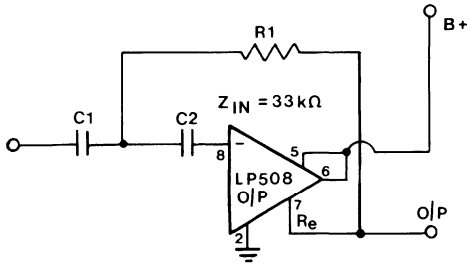
Output of the 508 is not an ideal op-amp therefore modifications are necessary when using the output stage as a buffer filter. The following diagrams show how this can be achieved.



$R1 = R2$
$C2 = 2C1$

$$f_c = \frac{1}{2 \times \pi \times R1 \times C1 \times \sqrt{2}}$$

Fig. 6 Active Buffer Low Pass Filter using a 508 Output Stage.



$$C1 = C2$$
$$R2 = 2R1$$
$$R2 = Z_{IN}$$
$$f_c = \frac{1}{2 \times \pi \times R1 \times C1 \times \sqrt{2}}$$

Fig. 7 Active Buffer High Pass Filter using a 508 Output Stage.

Note: 1) R1 and R2 must be 10 times less than Z_{IN} for low pass.
2) Collector output pin is tied to supply.

OTHER FEATURES

Both the LP and LC508 each have an internal 4k Ω microphone decoupling resistor.

With the addition of an external capacitor an effective decoupling network is achieved.

APPLICATION CIRCUITS

The circuit of Fig. 8 is an LC508 Class A Amplifier with the LV560 used as a digitally controlled volume control. The LV560 was designed to work around the feedback loop of a 508 preamp. Typically the impedance of the LV560 is adjustable between 4kΩ - 500kΩ (42dB). The gain of the LC508 preamp is calculated in the same manner as if a fixed resistor was used externally.

For more information on the LV560 Digitally Controlled Transconductance Block, refer to data sheet No.500 - 88 - 4.

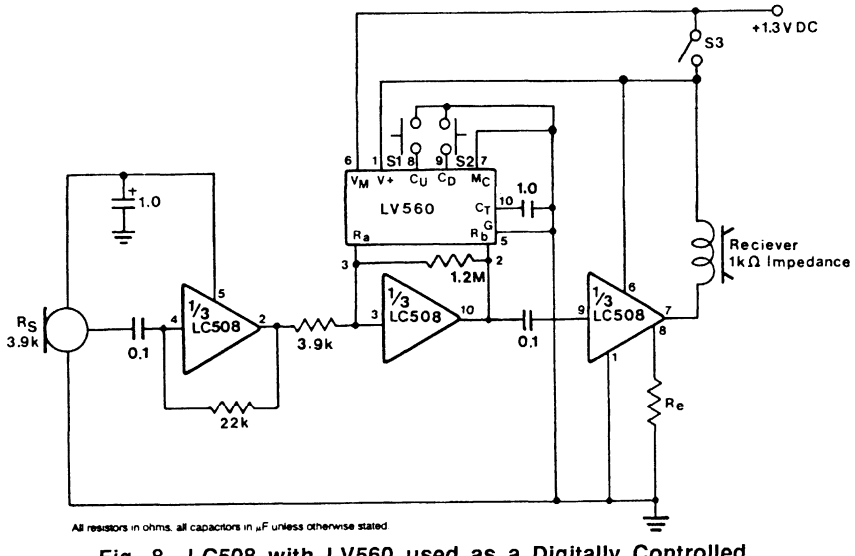
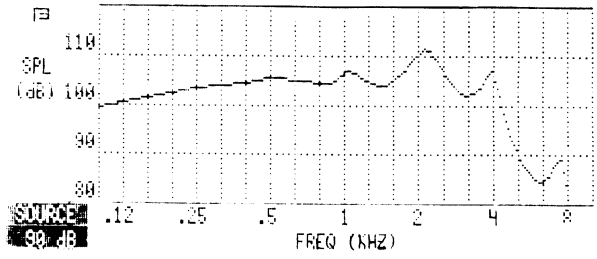


Fig. 8 LC508 with LV560 used as a Digitally Controlled Volume Control



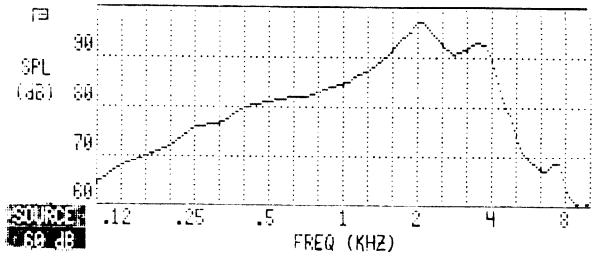
MAX OUTPUT
111.5 dBSPL
AT
2.120 KHZ

90 dB HF AVG
106.5 dB SPL

HF AVG
FULL ON GAIN
37.0 dB AT
60.0 dB SPL
INPUT

RESP. CURVE GAIN
29.5 dB

90 dB HF AVG-77=
29.5 dB

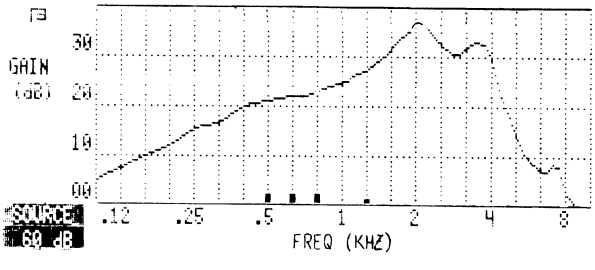


RESPONSE LIMIT: 69.5
F1: 0.151 KHZ
F2: 5.600 KHZ

TOTAL HARMONIC DIST:
0 % AT 0.5 KHZ
1 % AT 0.8 KHZ
0 % AT 1.6 KHZ

EQUIVALENT
INPUT NOISE
28.0 dB SPL

BATT. CURRENT
.44 MA AT
ZINC-AIR(1.30V)
SETTING WITH
65 dB SPL AND
1.000 KHZ INPUT



HF AVG:
89.5 dBSPL

EQUIVALENT
INPUT NOISE
31.0 dB SPL

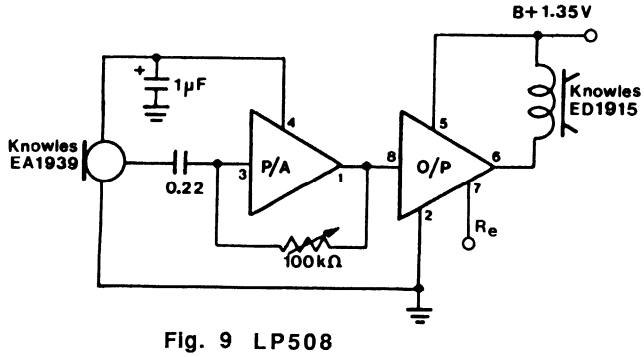
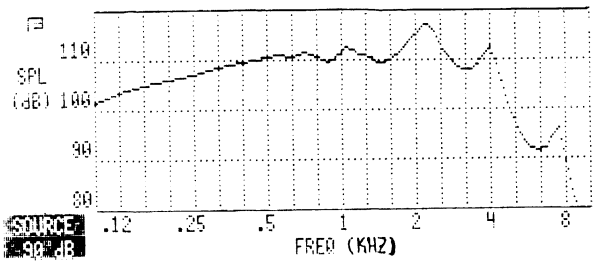


Fig. 9 LP508



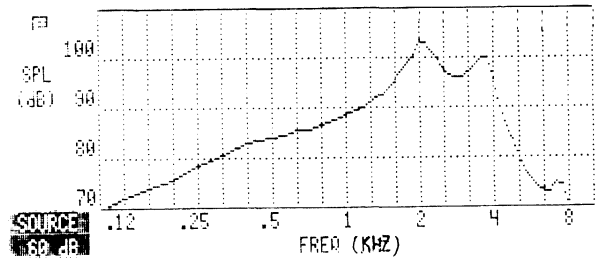
MAX OUTPUT
117.0 dBSPL
AT
2.240 KHZ

HF AVG
FULL ON GAIN
39.5 dB AT
60.0 dB SPL
INPUT

RESP. CURVE GAIN
34.0 dB

90 dB HF AVG
111.5 dB SPL

90 dB HF AVG-77=
34.5 dB

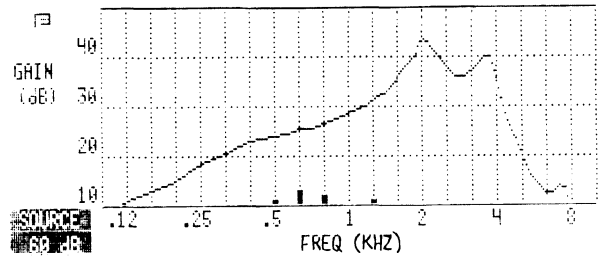


RESPONSE LIMIT: 74.0
F1: 0.160 KHZ
F2: 6.000 KHZ

EQUIVALENT
INPUT NOISE
28.0 dB SPL

BATT. CURRENT
.84 MA AT
ZINC-AIR(1.30V)
SETTING WITH
65 dB SPL AND
1.000 KHZ INPUT

TOTAL HARMONIC DIST:
1 % AT 0.5 KHZ
1 % AT 0.8 KHZ
Q% AT 1.6 KHZ



EQUIVALENT
INPUT NOISE
31.0 dB SPL

HF AVG:
94.0 dBSPL

Note: Acoustic responses for only the LP508 are shown because with the exception of higher gain similar responses can be achieved using the LC508.

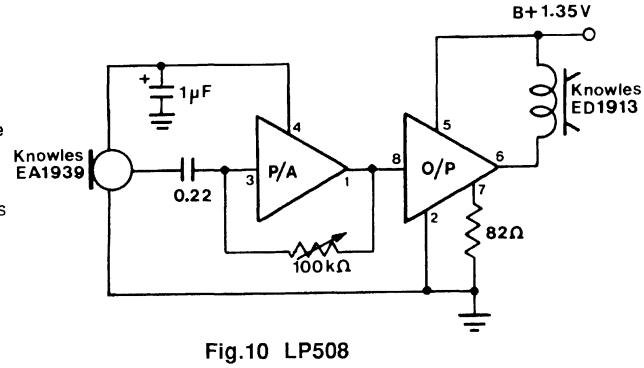


Fig.10 LP508

INTRODUCTION

This application note describes four methods of using the LD511 as a compression amplifier. The first three methods show the LD511 as a preamplifier in conjunction with the LC549 push-pull output amplifier. The last method illustrates how the LD511 can function as a "stand-alone" Class A compression amplifier.

This note provides basic suggestions which can be used by the circuit designer to develop circuits to meet his own particular needs, rather than to be an indepth study of compression circuits.

The LD511 as a Compressor

The LD511 is essentially a distortion free limiter in contrast to a peak clipping circuit, which is a high distortion limiter. However, both types of limiter provide compression. That is, they compress the input dynamic range into a narrower output dynamic range. At low input signal, the LD511 functions as a linear amplifier. As the input "threshold" is approached, the compression circuitry is activated and serves to hold the output constant despite further increases in input signal. The LD511 employs delayed automatic gain control to achieve its compression action.

COMPRESSION AMPLIFIER CIRCUITS

Method 1 - Limiting Output Constant

Fig. 1 shows a configuration in which gain and threshold are adjusted by a single potentiometer (VC) while the limited output remains constant. The compression characteristic resulting from this circuit is depicted in the graph of Fig. 1a.

Compression Characteristics

The terms input and output compression have been avoided in this note because of their varied interpretation. In addition, the use of these two terms implies that only two compression characteristics (being a graph of output vs input) are possible, whereas this note describes three types of compression characteristics (Fig. 4 being a version of Fig. 1).

In general, there are three important parameters which define the compression characteristic: gain, threshold, and limiting output. Each of these may be adjusted, usually by means of a variable resistor or potentiometer. In the relatively simple circuits described in this note, a single potentiometer (or variable resistor) is used to change two of the key parameters simultaneously, while the third remains fixed. The choice of circuit configuration therefore depends on the designer's objectives. A single design could incorporate multiple potentiometers and/or switching to achieve more than one type of characteristic.

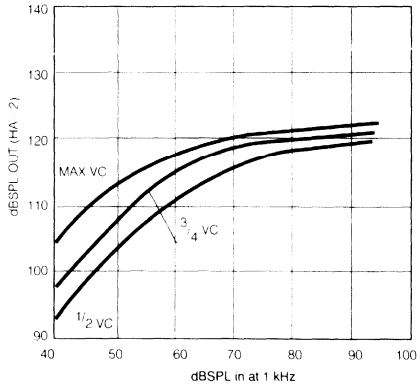


Fig. 1a

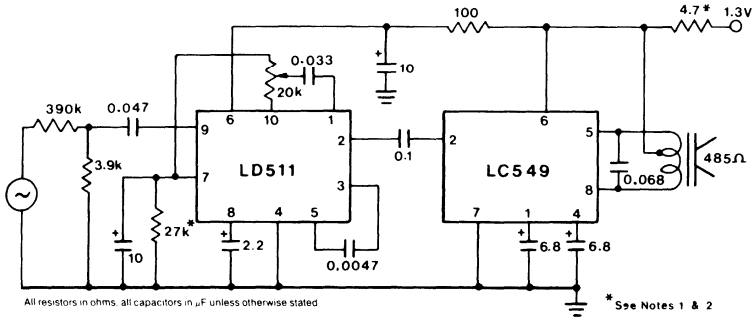


Fig. 1 Limiting Output Constant Circuit

BA 2

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Method 2 - Gain Constant

In Fig 2. a single potentiometer (R_T) adjusts threshold and limited output. Gain below threshold remains constant. The compression characteristic is depicted in the graph of Fig. 2a. The circuit in this example could be simplified by making R_T a 200 kΩ resistor between pin 2 and ground. However, this simplification reduces the possible range of compression characteristic adjustment.

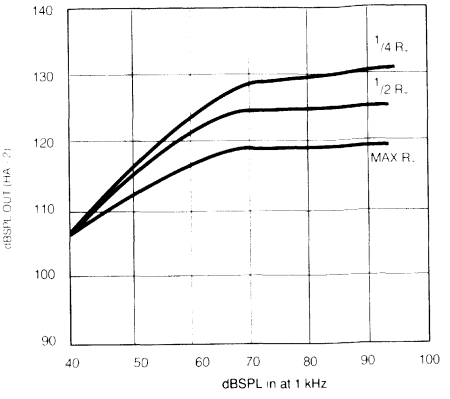
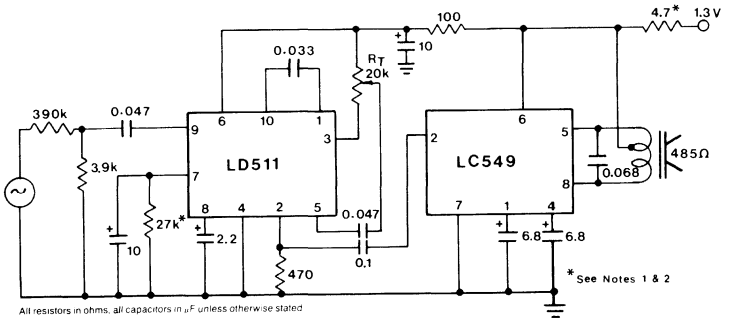


Fig. 2a

Fig. 2 Gain Constant Circuit



Method 3 - Threshold Constant

In Fig.3, a single VC potentiometer adjusts gain and limited output, while the threshold remains constant. The compression characteristic is shown in the graph of Fig. 3a.

A similar result can be achieved in Method 1, by adding a variable resistor R_T in series with pin 3. For example, an additional family of curves with a limiting output at 130 dBSPL can be generated.

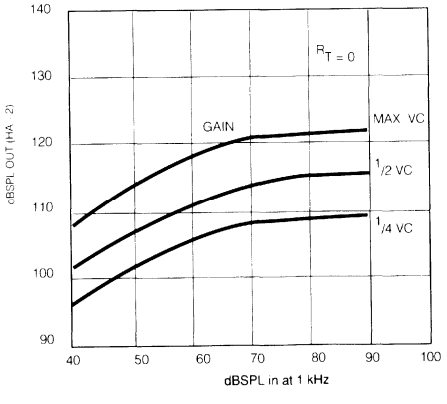
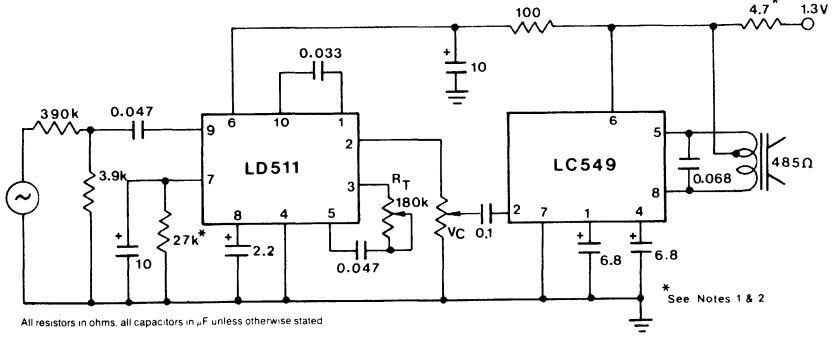


Fig. 3a

Fig. 3 Threshold Constant Circuit



As an example of the flexibility in this method, the graph of Fig. 3b shows the effect of adding a variable resistor R_T in series with pin 3 of the LD511. For every value of R_T, a completely new family of curves can be generated which are identical in shape to those of Fig. 3a, but for which the maximum value of the limiting output has been increased.

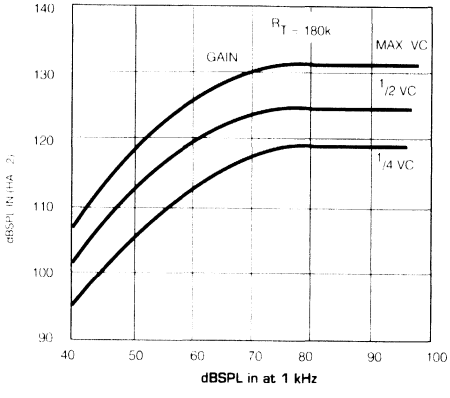


Fig 3b

Method 4 - The LD511 as a "Stand-Alone" Class A Compression Amplifier

This circuit example shows the LD511 as a "stand-alone" Class A compression amplifier driving a 1000 Ω receiver. The characteristics obtained from this configuration will be similar to those of Method 1. That is, gain and threshold are adjusted by a single VC potentiometer and limiting output remains constant. Increased flexibility can be obtained by adding variable resistor R_T. This will allow adjustment of the limiting output independent of the effects of VC.

When used as a "stand - alone" Class A compression amplifier, the LD511 is essentially similar in performance to the LD501. For this reason, Application Note No. 500 - 24, *The 501 as Input and Output Compression Amplifier*, can be utilized for further development of LD511 circuits.

Notes:

1. The 4.7Ω resistor shown in series with the 1.3 V supply in Figures 1,2,3 and 4 is intended only to simulate the source impedance of a typical battery for test purposes. This resistor should be omitted in actual hearing aid designs.

2. In Methods 1,2 and 3, the 27kΩ resistor from pin 7 to ground serves to simulate the DC current drain of a typical electret microphone. This resistor should be omitted in actual hearing aid designs.

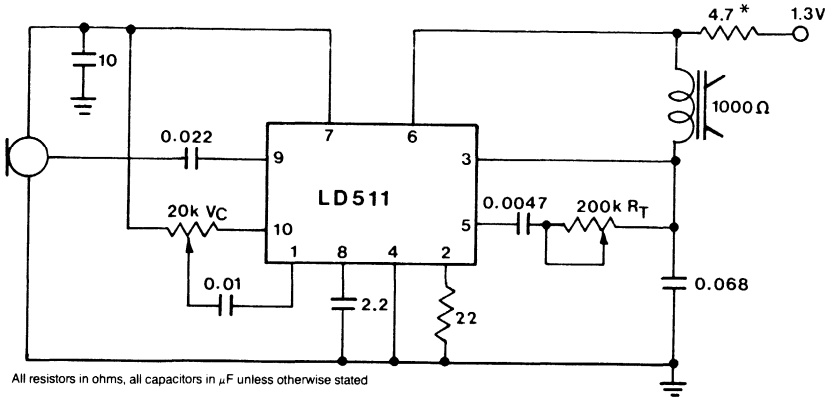


Fig. 4 LD511 as a Stand-Alone, Class A Compression Amplifier

GENNUM CORPORATION

Input Compression Amplifier System - LD511

APPLICATION NOTE

INTRODUCTION

This note describes the application of the LD511 in combination with a single external amplifier to produce a highly flexible input compression Class A system for ITE and BTE aids.

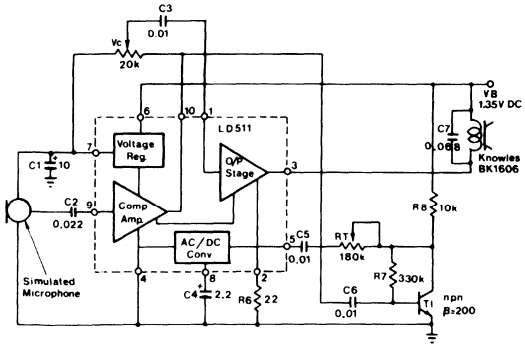
The term input compression implies a delayed AGC (automatic gain control) system, where the feedback is taken between the preamp output and the volume control. This results in having the volume control simultaneously adjust the gain and the maximum output, while the threshold level, determined by AGC, remains unaffected.

The input compression circuit with the LD511 was quite suitable for behind-the-ear or in-the-ear hearing aids. *Input compression* requires that only four additional components are required to be connected to the typical stand alone LD511 amplifier.

The LD511 input compression was tested in the BTE configuration. With the compression disconnected, a maximum output of 123 dBSPL peak and a gain of 50 dB peak was achieved. With compression active, the volume control (VC) and threshold trim resistor (R_T) can be adjusted to provide a wide range output and threshold levels.

HEARING AID CIRCUIT

The LD511 was initially designed as an output compression amplifier. Its flexibility allows it to be incorporated in an input compression system with the addition of an external transistor T1 and its associated components (R7, R8 and C6) shown in Figure 1.



All capacitors in pF, all resistors in ohms unless otherwise stated.

Fig.1 Input Compression Hearing Aid Circuit

Transistor T1 is used as the AGC amplifier which has a gain of 25 dB. Its input is coupled via capacitor C6 to the output of the LD511 compression amplifier. As such, the volume control VC is outside the feedback loop and provides the input compression characteristic depicted in Figure 2. The output of the volume control is coupled via capacitor C3 to the LD511 output stage at pin 1. This output stage drives a two terminal receiver such as the Knowles BK1606 or equivalent. If other receivers with different impedances are used, the bias current can be adjusted by resistor R6 connected to pin 2.

By connecting C6 to the volume control centre tap instead of pin 10, the circuit of Figure 1 can be converted to an output compression system. Its characteristics will be similar to those of a 'Stand-alone' Output Compression Amplifier, see Application Note 500-35. The principle difference being that the feedback signal which activates the AGC amplifier is derived from a linear resistive load rather than from the frequency dependent inductive receiver. A much smoother compression active frequency response will result

HEARING AID PERFORMANCE

The acoustic performance of the LD511 input compression system is shown in Table 1.

PARAMETER	VALUE	UNITS	CONDITIONS
Supply Voltage	1.35	V DC	
Total Current	1.45	mA	
Acoustic Output	110	dBSPL	60dBSPL I/P at 1kHz
Max.Acoustic O/P	123	dBSPL	90dBSPL 1/P at 1kHz
Acoustic Gain	50	dB	60dBSPL I/P at 1kHz
H.F. Average SSPL90	117.6	dB	
Attack Time		3	ms
Release Time		45	ms
Volume Control Range	∞		

Table 1 Acoustic Performance

Note: The above data was measured using the circuit arrangements depicted in Figure 1.

BA 3

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The receiver was coupled into 32 mm of No. 15 and 25 mm of No. 13 tubing into a HA-2 coupler connected to a B&K 2203 sound level meter.

The attack and release times of the circuit were measured at 3 ms and 45 ms respectively; they are adjusted by increasing or decreasing the value of C4 which will increase or decrease the attack and release times. The ratio of the attack and release times will remain constant at 1:15, independent of C4.

Figure 2 shows the transfer characteristic of the compression hearing aid for two settings of the volume control. Note that adjustment of the volume control adjusts both gain and maximum output simultaneously, while the input threshold or knee point remains unaffected. This is typical of all input compression systems, whatever the circuit employed.

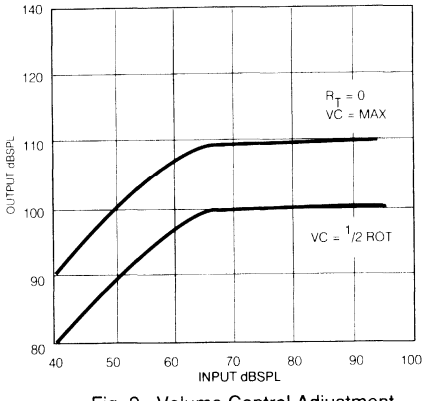


Fig. 2 Volume Control Adjustment

The results in Figure 3 show the effect of R_T on the transfer characteristic. Changing R_T from 0 Ω to 200 kΩ achieves a threshold shift of 10 dB. This is accompanied by a similar increase in maximum output with this gain remaining constant. If the value of R_T is greater than 200 kΩ, the amplifier will saturate due to its own output limitations even before the AGC is activated. If this happens, both the value and predictability of the attack and release times and their ratio will be substantially different to those reported in Table 1.

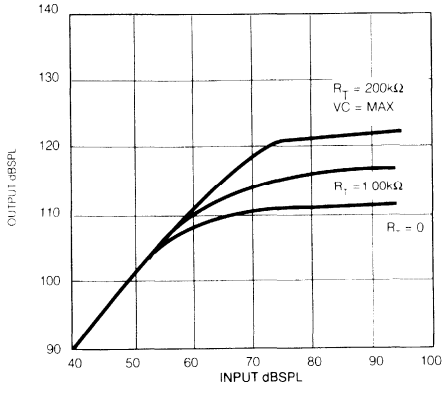


Fig. 3 Compression Threshold Adjustment

Figure 4 depicts the hearing aid frequency response with both the compression inactive (Response A) and compression active (Response B). This data was measured using the test arrangement of Figure 1. The input signal was mixed with a pink noise* source and set to an equivalent input level of 70 dB SPL. The output was measured using a tuneable narrow band notch filter (Q = 20) followed by a level detector.

**Pink noise is broadband noise whose energy decreases with increasing frequency at the rate of 3 dB/octave. It is more representative of 'real life' signals than a pure tone.*

Apart from a difference in gain, Response A and Response B are very similar in shape which indicates that the circuit components have been optimized for the desired low frequency response.

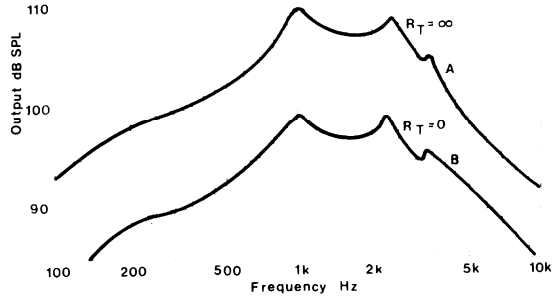


Fig. 4 Frequency Response with Compression Inactive (A) and Active (B)

SETTING THE HEARING AID LOW FREQUENCY RESPONSE

Determining the low frequency response on a single channel input (or output) compression hearing aid requires a deliberate compromise between frequency response, discrimination and distortion.

If an extended low frequency response is utilized, then listening situations which involve ambient noise with high energy may activate the AGC circuitry and depress the gain of the hearing aid. Desired information at higher frequencies will receive too little amplification with consequent degradation in discrimination. A partial solution to this problem is to use C6 (Figure 1) to filter low frequency signals out of the AGC circuitry. This will prevent gain reduction with the presence of low frequencies but may lead to overload of the output stages of the amplifier which will distort the desired information signal. A safer approach is to select C2 to attenuate low frequency signals before they enter the amplifier.

A suggested method for optimizing C2, C4 and C6 is as follows:
(a) With the compression loop deactivated (R_T = 1) and using a pure tone inputof 80 dBSPL select C2 to obtain the desired low frequency response.

(b) With the compression loop activated (R_T = 0) and C4 = 10µF, compare the compression activated and deactivated frequency response. Reduce the value of C6 until a slight boost in the compression active frequency response occurs.

(c) Select C4 to obtain the desired release time. To prevent distortion due to too short a release time, C4 should be adjusted to provide a release time at least five times the period of the frequency at which the boost was observed. For example, for low distortion at 200 Hz, a release time of at least 25 ms is required.

LD511 INPUT COMPRESSION AS A LOW FREQUENCY SIGNAL PROCESSOR

Since the compression function of the LD511 is frequency dependent, the LD511 can also be used as a type of signal processor whether it be input or output compression. With proper component selection, the LD511 will automatically adjust the gain of the low frequencies when noise and speech are present.

This is accomplished by having the output of T1 (Figure 1) fed back through a coupling capacitor C5 into an AC/DC converter rectifying the AC signal. This DC voltage is then filtered by C4 and the level of the DC voltage determines the gain of the first stage. Therefore, if the output voltage is high, the signal feedback and the DC level from the rectifier is high and the gain of the first stage is reduced. The threshold at which this occurs is controlledby R_T.

With the AGC feedback being frequency dependent, low frequencies are attenuated by the combination of C5 and the input impedance of the AC/DC converter. Since the input impedance is fixed, C5 solely determines the low frequency gain.

If C5 is set to 0.001 µF, the break point at which the low frequency rolls off the AGC feedback amplifier becomes 1.2 kHz. Thus any frequency above1.2 kHz will activate the AGC, decreasing the gain.

Figure 5 shows how the low frequency gain is affected when a pure tone sweep is mixed with a fixed frequency. Curve 1 is the response of the hearing aid with a pure tone frequency sweep without any other signal mixed in.

Curve 1 - pure tone swept frequency
2 - pure tone swept frequency mixed with 500 Hz
3 - pure tone swept frequency mixed with 1 kHz
4 - pure tone swept frequency mixed with 3 kHz
5 - pure tone swept frequency mixed with 4 kHz

If the maximum low cut response is required, the measurement can be made by using a pure tone sweep with a pink noise as depicted in Figure 6.

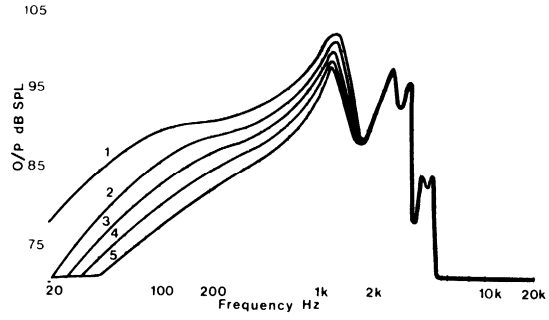


Fig. 5 Acoustic Frequency Response of LD511

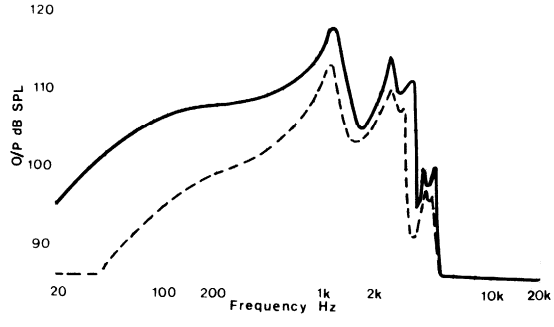


Fig. 6 Low Frequency Signal Processor BTE Acoustic of LD511 Frequency Response I/P Compression.

It should also be noted that the feedback capacitor C5 be carefully chosen, because if it is too large in value, the low frequency gain will be greater than the bandpass gain using a pure tone sweep. This would allow the low frequency signal to overload the hearing aid, especially if there was no speech present to decrease the low frequency gain of the circuit.

BA 3

Designing with the Adaptive High Pass Filter LS581, LF581

APPLICATION NOTE

DESCRIPTION

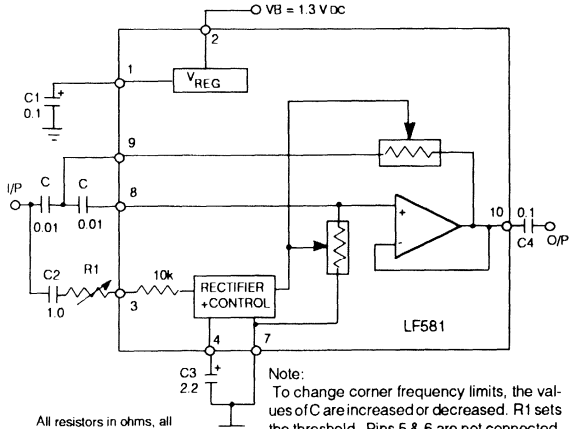
The LF / LS581 is a unity gain adaptive 12 dB/oct highpass Butterworth filter. The filter corner frequency varies from 200 Hz to 2 kHz, as the background noise level increases 20 dB above a predetermined threshold level of the internal rectifier. Once the noise level has increased 20 dB above the threshold, no further changes in the corner frequency will occur.

There are two versions of the 581. The LF581 (Figure 1), consists of a filter, voltage regulator and a rectifier while the LS581 (Figure 2), contains an added preamplifier.

Designing with the 581 allows two options for placement of the filter section. It can be placed immediately after the microphone output or following a preamplifier. This choice is possible due to an input dynamic range of approximately 86 dB, based upon its typical noise floor level of 3 µV and large signal handling level of 65 mV at 5% distortion.

The rectifier on the 581 controls the position of the corner frequency of the filter. It has a typical input threshold of 2.5 mVRMS before it begins to adjust the corner frequency. Since 2.5 mVRMS input corresponds to 82 dBSPL (using a microphone with a sensitivity of -60 dBV / µB at 1 kHz) a preamplifier is required to lower the threshold to 60 dBSPL INPUT. Thus the 581 is required to have at least 20 dB of preamplification in front of the rectifier for operation. This preamplifier is available on the LS581 while the LF581 requires a separate preamplifier. The preamplifier on the on the LS581 is an inverting op-amp with a typical open loop gain of 45 dB. A 265 kΩ resistor is connected across the preamplifier to simplify gain setting and to reduce external components.

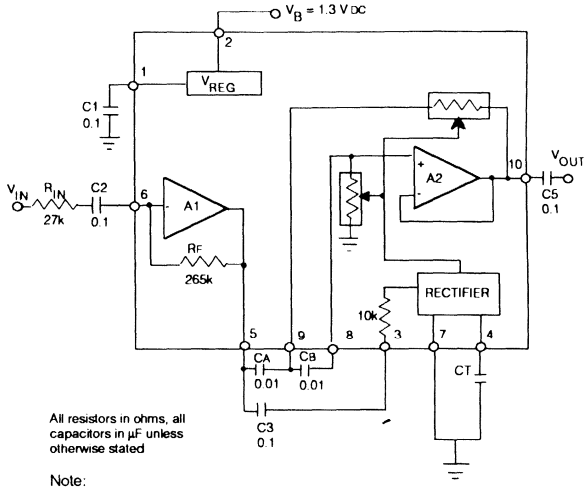
Fig.1 LF581 Block Diagram



All resistors in ohms, all capacitors in µF unless otherwise stated

Note:
To change corner frequency limits, the values of C are increased or decreased. R1 sets the threshold. Pins 5 & 6 are not connected. Electrical input determined by using a microphone with a sensitivity of -60 dB/µB @ 1Hz

Fig. 2 LS581 Block Diagram



All resistors in ohms, all capacitors in µF unless otherwise stated

Note:
To change corner frequency limits, the values of C are increased or decreased. R1 sets the threshold. Pins 5 & 6 are not connected. Electrical input determined by using a microphone with a sensitivity of -60 dB/µB @at1Hz

THEORY OF OPERATION

The LF/LS581 adaptive filter is designed to remove low frequency noise in the presence of speech. This is accomplished by using an adaptive filter with a varying corner frequency from 200 Hz to 2 kHz. The corner frequency location of the filter, depends upon two conditions. The first is that the signal must exceed a predetermined threshold, set by the preamplifier into the rectifier. The second is the periodic duration of the incoming signal. The latter is the most important condition because it is this characteristic which differentiates between short term average speech and long term average noise.

The differentiation between speech and noise is accomplished by the setting of the attack time on the rectifier. With the attack time set to 30 ms or higher, the filter will not react as much to short term average speech frames less than 30 ms, but will be more responsive to relatively stationary background noise, which has a long term average level.

Once the rectifier has sensed the noise, the actual position of the filter corner frequency is dependent upon how far the noise level has exceeded the threshold level. This detection method provides a wideband response for speech and a narrow band for noise when present.

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This characteristic of differentiation of noise from speech is shown in the following figures.

Figure 3 illustrates the frequency response of the filter measured at 3 input levels, 60 dBSPL, 70 dBSPL and 80 dBSPL. Pink noise is used as a source to simulate noisy conditions. Since the input is a constant noise the filter will always react to the signal once it is above the rectifier threshold. At 60 dBSPL IN the corner frequency of the filter begins at 200 Hz, while at 70 dBSPL IN it begins at 700 Hz and at 80 dBSPL IN, the corner frequency is at 2 kHz.

To demonstrate that the 581 is not as sensitive to speech as it is to noise a simulated speech pulse is used as a test signal which simulates the temporal characteristic of speech. This speech weighted signal is filtered from 200 Hz to 4 kHz and it has a time period of 30 ms, see Figure 4.

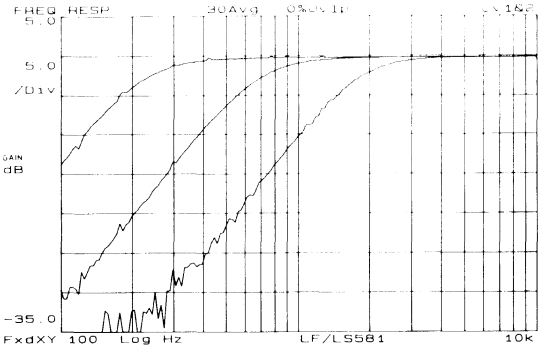


Figure 3

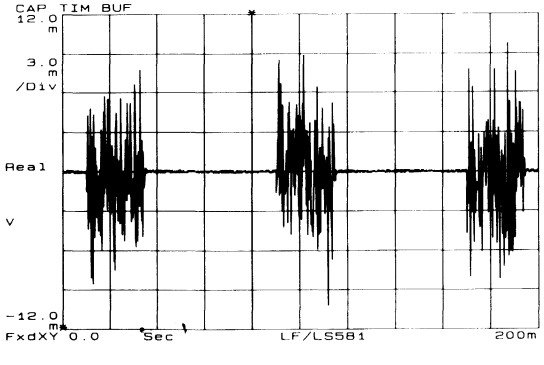


Figure 4

By applying the speech weighted signal to the input of the filter at a level equivalent to 70 dBSPL, a dual channel FFT analyser is used to extract the frequency response of the 581 filter and it is compared to the response of the filter with a pink noise input, also at 70 dBSPL IN, see Figure 5.

The input levels for the speech weighted signal and pink noise are then increased to 80 dBSPL, with the resultant frequency response shown in Figure 6. Notice that the frequency response of the speech weighted signal has increased slightly from Figure 5 to Figure 6. This is because the 581 filter, as previously stated, is also effected by signals exceeding the rectifier input threshold. However since it is pulsed noise, the average signal level is lower than that of the average signal level of pink noise at the same peak level.

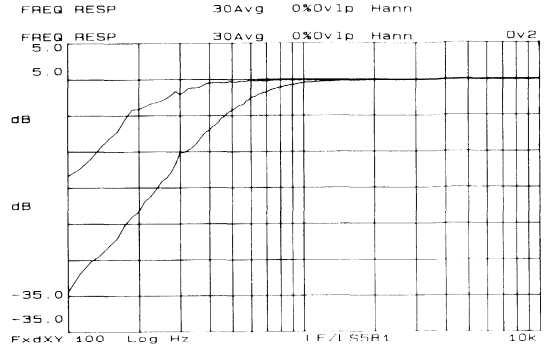


Figure 5

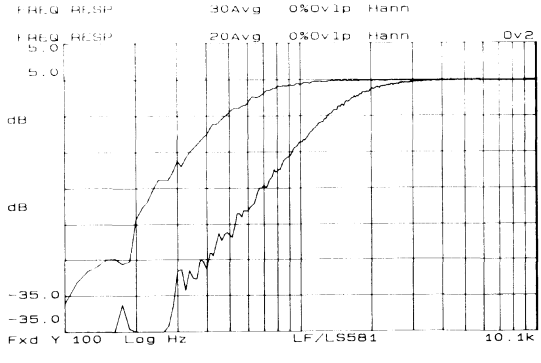


Figure 6

APPLICATION CIRCUITS

The LF/LS581 will operate in conjunction with linear amplifiers or compression amplifiers, and is compatable with a variety of output stages.

For the linear configuration, which is also the lowest parts count circuit, the LS581 could be combined with the LS505 as shown in Figure 7. It is important that the gain of the preamplifier to the 581 rectifier be set to approximately 20 - 25 dB, in order to set the threshold to 60 dBSPL or as required

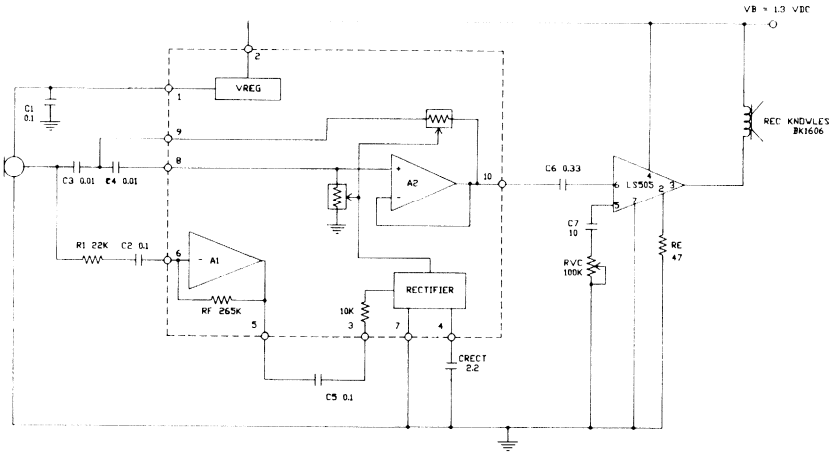


Fig. 7 LS581/LS505
Typical Application Circuit

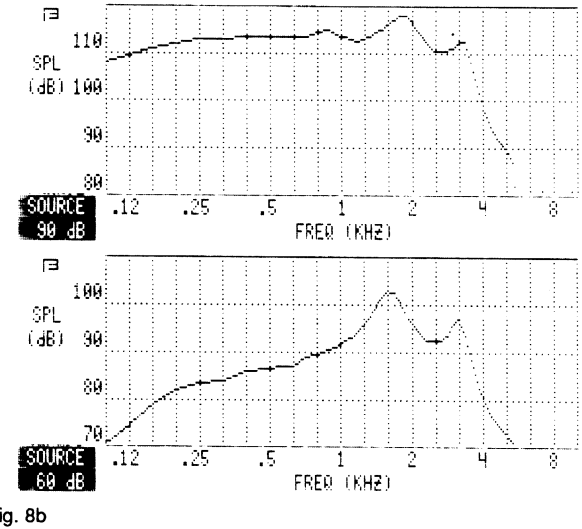


Fig. 8a

MAX OUTPUT
118.0 dBSPL
AT
1.900 KHZ

90 dB HF AVG
113.5 dB SPL

RESPONSE LIMIT: 76.0
F1: 0.136 KHZ
F2: 4.438 KHZ

TOTAL HARMONIC DIST:
1 % AT 0.5 KHZ
% AT 0.8 KHZ
1 % AT 1.6 KHZ

HF AVG
FULL ON GAIN
54.0 dB AT
60.0 dB SPL
INPUT

RESP. CURVE GAIN
36.0 dB
90 dB HF AVG-77=
36.5 dB

EQUIVALENT
INPUT NOISE
27.5 dB SPL

BATT. CURRENT
1.12 MA AT
ZINC-AIR(1.30V)
SETTING WITH
65 dB SPL AND
1.000 KHZ INPUT

Fig. 8b

Figures 8a,b,c Acoustic Performance Graphs of the LS581/LS505

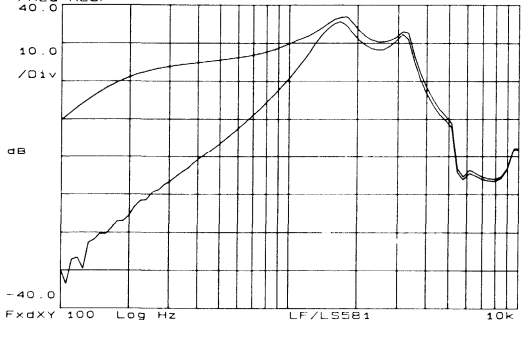


Fig. 8c

Since the LF / LS581 filter section is unity gain, inserting it into an existing application such as the LS505 will not effect the HFA gain of the LS505 hearing aid circuit, providing that the gain is measured when the filter has its corner frequency at its lowest point of 200 Hz. The acoustic performance of the LS581 / LS505 is shown in Figure 8.

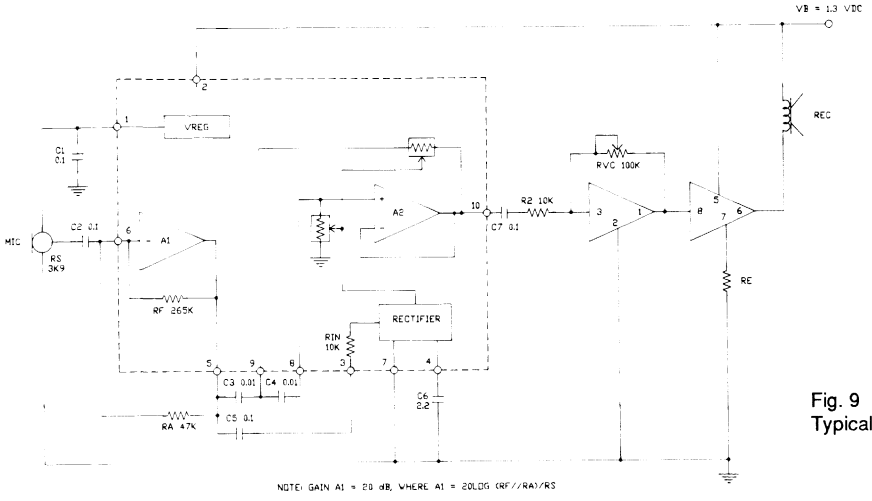
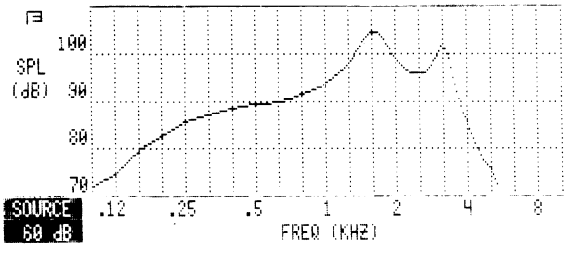


Fig. 9 LP508/LS581
Typical Application Circuit



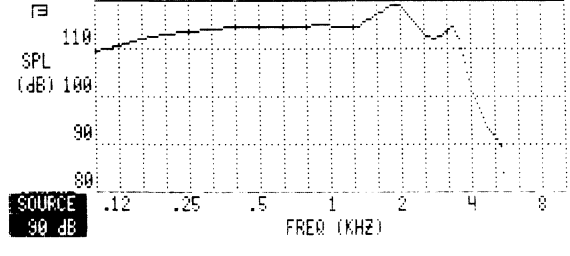
RESPONSE LIMIT: 78.0
F1: 0.149 KHZ
F2: 4.650 KHZ

EQUIVALENT
INPUT NOISE
25.0 dB SPL

BATT. CURRENT
1.16 MA AT
ZINC-AIR(1.30V)
SETTING WITH
65 dB SPL AND
1.000 KHZ INPUT

TOTAL HARMONIC DIST:
1 % AT 0.5 KHZ
% AT 0.8 KHZ
1 % AT 1.6 KHZ

Fig. 10a



MAX OUTPUT
119.0 dBSPL
AT
2.000 KHZ

HF AVG
ULL ON GAIN
52.0 dB AT
60.0 dB SPL
INPUT

ESP. CURVE GAIN
38.5 dB

90 dB HF AV
115.0 dB SPL

0 dB HF AVG-77=
38.0 dB

Fig. 10b

Figures 10a,b,c Acoustic Performance Graphs of the LP508/LS581

For an improved version where the gain of the hearing aid circuit can be trimmed, the LS581 can be combined with the LP508, Figure 9, with the corresponding acoustic curves shown in Figure 10.

If compression is required to limit high input transients, combine the LS581 with the LD511 (Fig.11) for output compression , or the LF581/LD502/LC508 (Fig.12), and the LS581/LD512 (Fig. 13) for input compression.

It is not recommended that the compression amplifier drive the LF/LS581 rectifier, because the gain of the compression amplifier is dependent upon the input signal level.

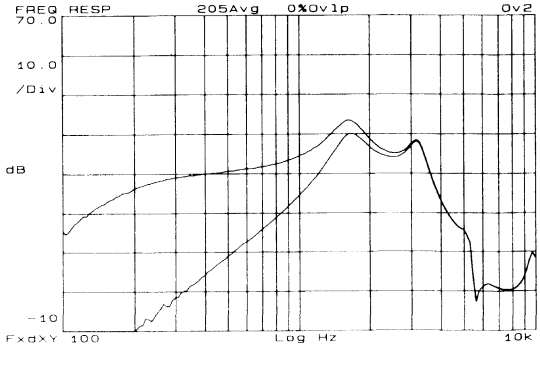


Fig. 10c

Since the gain of the compression amplifier is changing, the threshold of the 581 rectifier will not be constant. Instead, a linear preamplifier, such as the LS581 preamplifier or a section of the LC508, should be used to drive the rectifier control circuitry, making the threshold on the 581 independent of the gain of the compression amplifier.

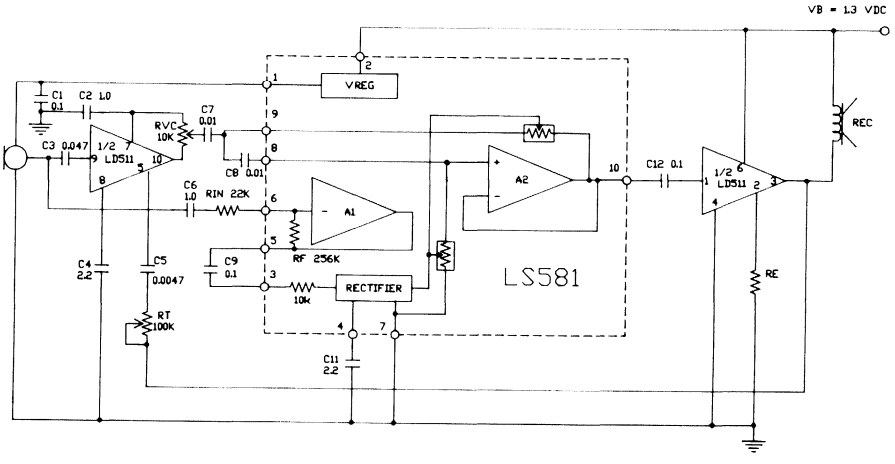


Fig. 11
LS581/LD511
Typical Application
Circuit (for output
compression)

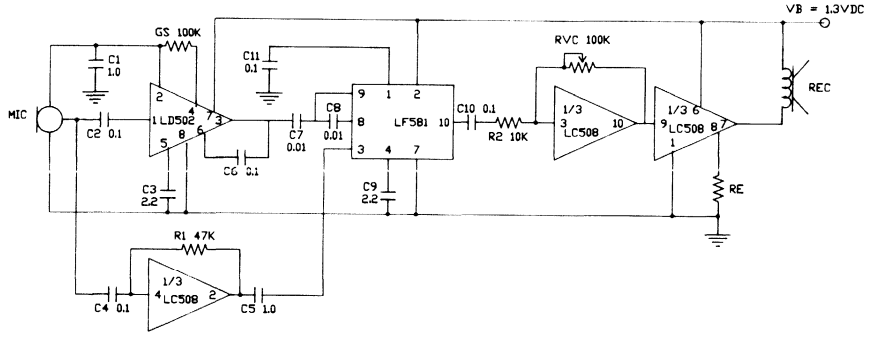


Fig. 12
LF581/LD502/LC508
Typical Application
Circuit (for input
compression)

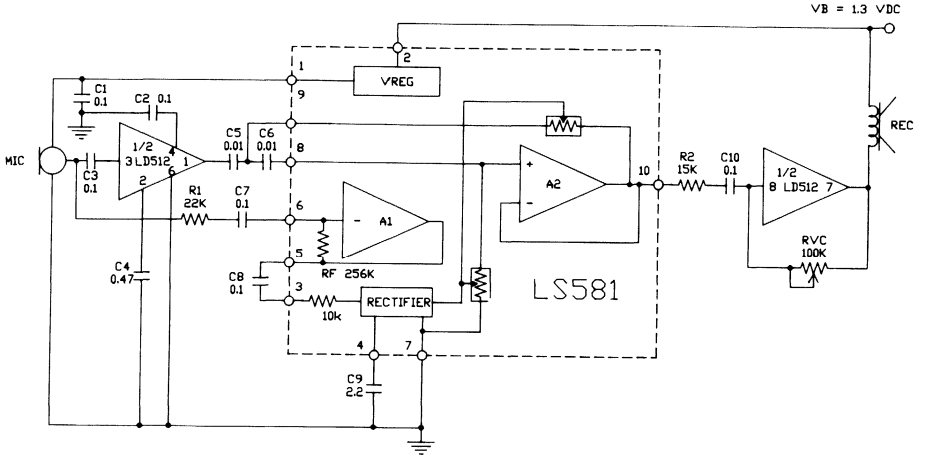


Fig. 13
LS581/LD512
Typical Application
Circuit (for input
compression)

G	GENNUM CORPORATE INFORMATION & SELLING POLICY AVAILABLE PACKAGING RELIABILITY THROUGH QUALITY
VBD	VIDEO & BROADCAST DATA SHEETS
VBA	VIDEO & BROADCAST APPLICATION NOTES
RMD	RESONANT MODE CONTROLLER DATA SHEETS
RMA	RESONANT MODE CONTROLLER APPLICATION NOTES
SPD	SPECIAL PRODUCTS DATA SHEETS
SCD	SEMICUSTOM IC ARRAY DATA SHEETS
BD	BiFET PRODUCTS DATA SHEETS
BA	BiFET PRODUCTS APPLICATION NOTES